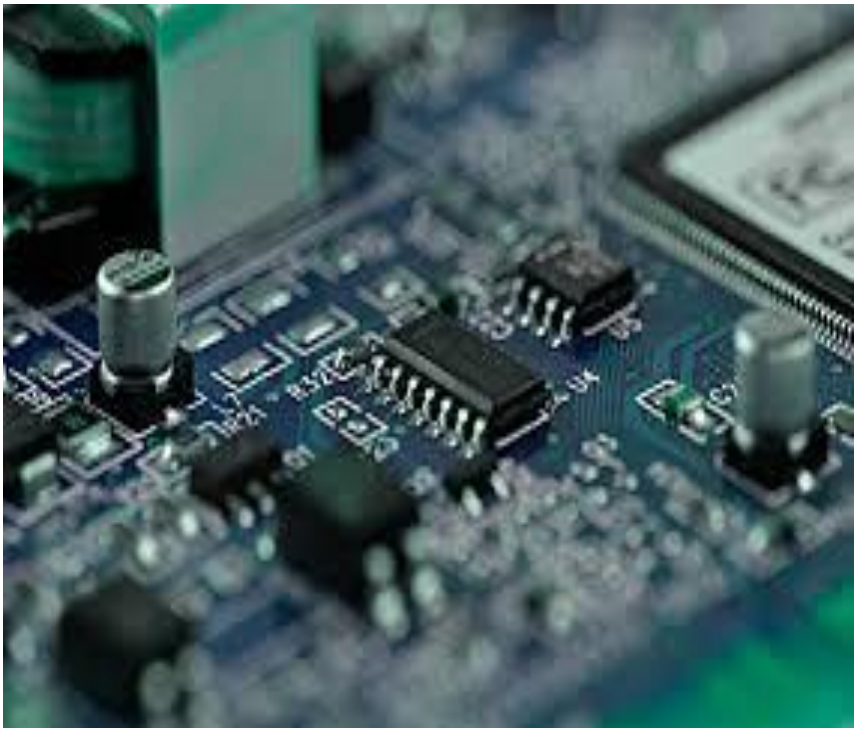


ELECTRONICS

Computer Techniques Engineering

Second year

Prepared by:
Mr. Saif Kamil

Electronics Fundamentals

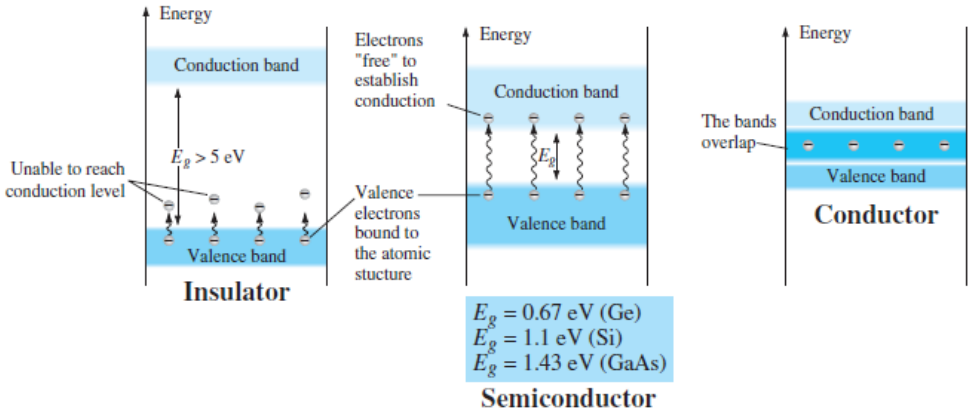
Electronics: branch of physics and electrical engineering that deals with the emission, behavior, and effects of electronics and electronic devices. The science and technology of the conduction of electricity in a vacuum, a gas, of a semiconductor, and devices based on them.

We know that some solids are good conductors of electricity while others are insulators. There is also an intermediate class of semiconductors. The difference in the behavior of solids as regards their electrical conductivity can be beautifully explained in terms of energy bands. The electrons in the lower energy band are tightly bound to the nucleus and play no part in the conduction process. However, the valence and conduction bands are of particular importance in ascertaining the electrical behavior of various solids.

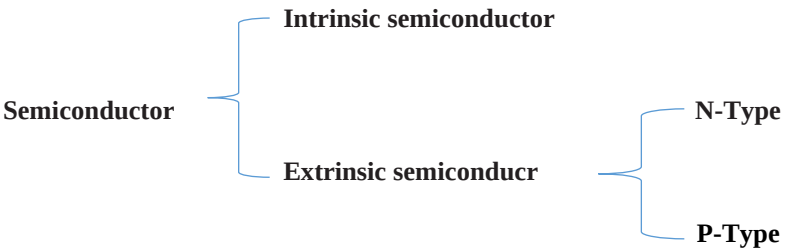
(i) Insulators: Insulators (e.g. wood, glass etc.) are those substances which do not allow the passage of electric current through them.

(ii) Conductors: Conductors (e.g. copper, aluminium) are those substances which easily allow the passage of electric current through them. It is because there are a large number of free electrons available in a conductor.

(iii) Semiconductors: Semiconductors (e.g. germanium, silicon etc.) are those substances whose electrical conductivity lies in between conductors and insulators. In terms of energy band, the valence band is almost filled and conduction band is almost empty. Further, the energy gap between valence and conduction bands is very small. Therefore, comparatively smaller electric field (smaller than insulators but much greater than conductors) is required to push the electrons from the valence band to the conduction band.



Types of semiconductors



1-Intrinsic Semiconductor

An intrinsic semiconductor is one which is made of the semiconductor material in its extremely pure form. Examples of such semiconductors are pure germanium and silicon.

2-Extrinisic semiconductor

Those intrinsic semiconductors to which some suitable impurity or doping agent or doping has been added in extremely small amount are called extrinsic or impurity semiconductors. Depending on the type of doping material used, extrinsic semiconductors can be divided into two types:

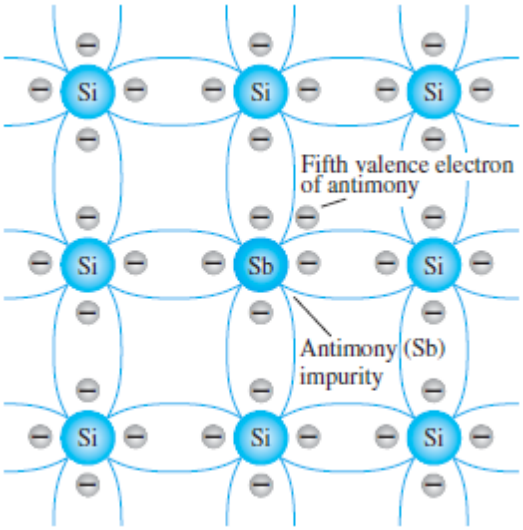
i- **N-Type semiconductor**

ii- **P-Type semiconductor**

N-Type semiconductor

Both *n* -type and *p* -type materials are formed by adding a predetermined number of impurity atoms to a silicon base. An *N*-type material is created by introducing impurity elements that have *five* valence electrons (*pentavalent*), such as *antimony*, *arsenic*, and *phosphorus*.
Note that the four covalent bonds are still present. There is, however, an additional fifth electron due to the impurity atom, which is *unassociated* with any particular covalent bond. This remaining electron, loosely bound to its parent (antimony) atom, is relatively free to move within the newly

formed *N*-type material. Since the inserted impurity atom has donated a relatively "free" electron to the structure: ***Diffused impurities with five valence electrons are called donor atoms.***

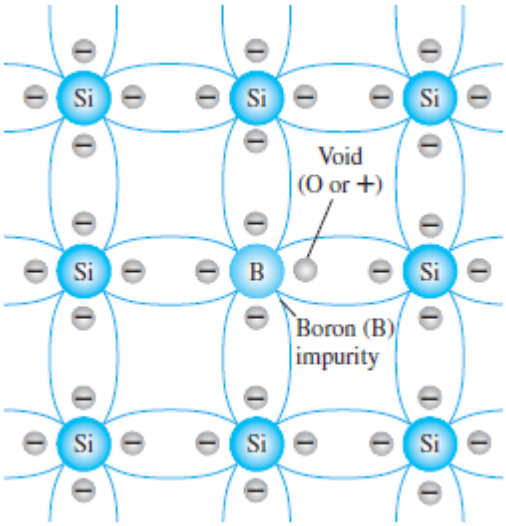


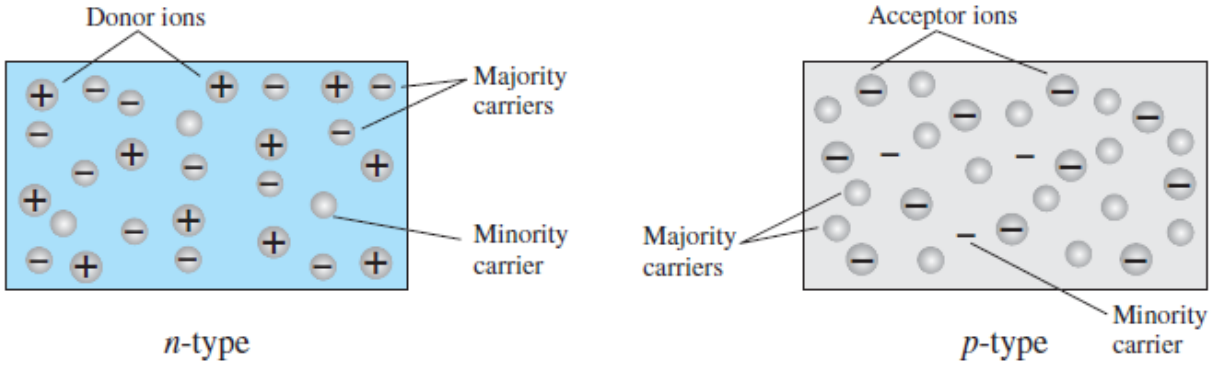
***P*-Type semiconductor**

The *p* -type material is formed by doping a pure germanium or silicon crystal with impurity atoms having *three* valence electrons. The elements most frequently used for this purpose are *boron, gallium,* and *indium*. Each is a member of a subset group of elements in the Periodic Table of Elements referred to as Group III because each has three valence electrons.

The effect of one of these elements, boron, on a base of silicon Note that there is now an insufficient number of electrons to complete the covalent bonds of the newly formed lattice. The resulting vacancy is called a *hole* and is represented by a small circle or a plus sign, indicating the absence of a negative charge. Since the resulting vacancy will readily *accept* a free electron:

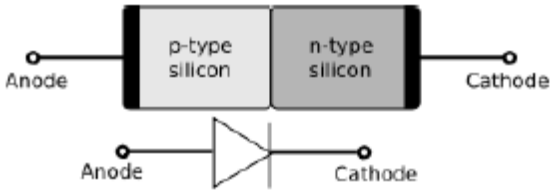
The diffused impurities with three valence electrons are called acceptor atoms.

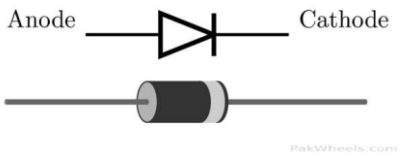




P-N Junction Diode

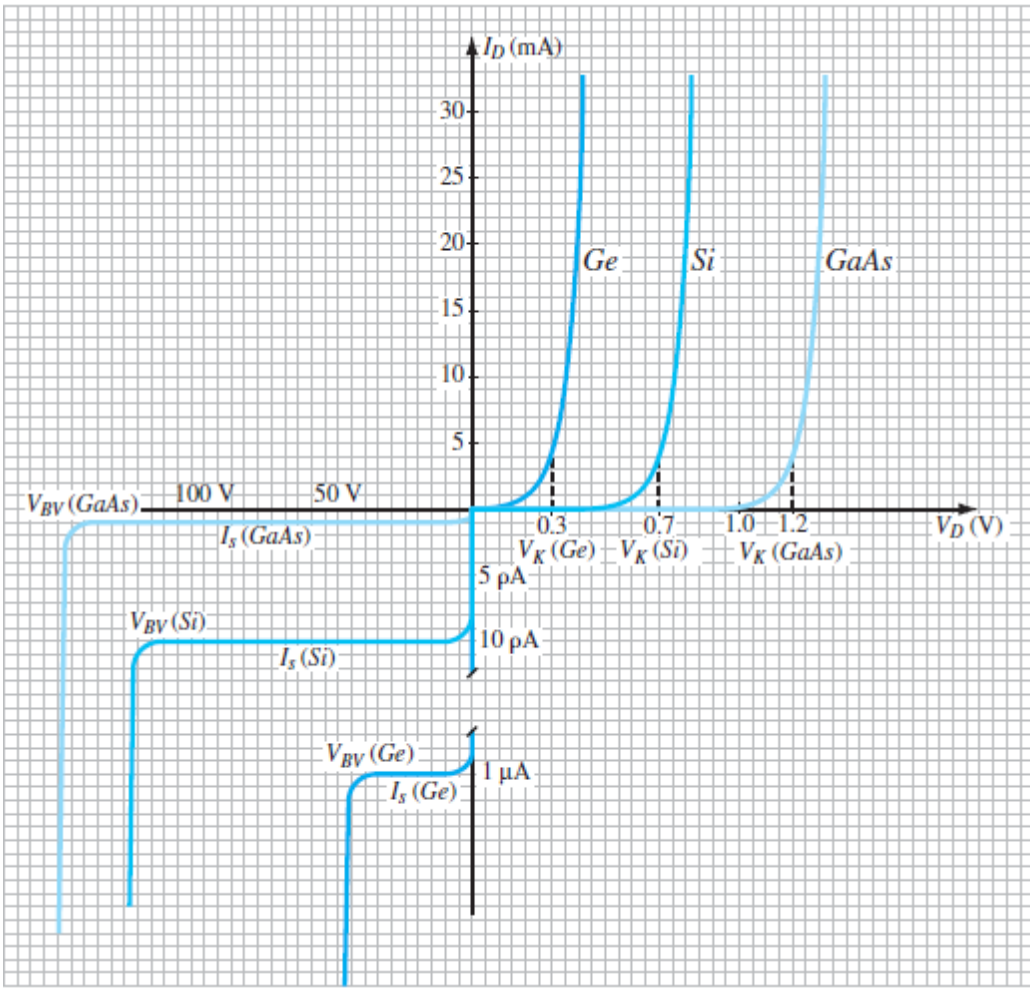
Now that both *n* - and *p* -type materials are available, we can construct our first solid-state electronic device: The *semiconductor diode*, with applications too numerous to mention, is created by simply joining an *n* -type and a *p* -type material together, semiconductor junction diodes are made by joining two semiconductors together. A P-N junction diode is formed by joining a P-type semiconductor to an N-type semiconductor. The basic simplicity of its construction simply reinforces the importance of the development of this solid-state era.





V/I characteristic

The figure shows the static voltage – current characteristic for the P-N junction diode.



It can be demonstrated through the use of solid-state physics that the general characteristics of a semiconductor diode can be defined by the following equation, referred to as Shockley's equation, for the forward- and reverse-bias regions:

$$I_D = I_S(e^{kV_D/T_K} - 1)$$

where *Is* is the reverse saturation current

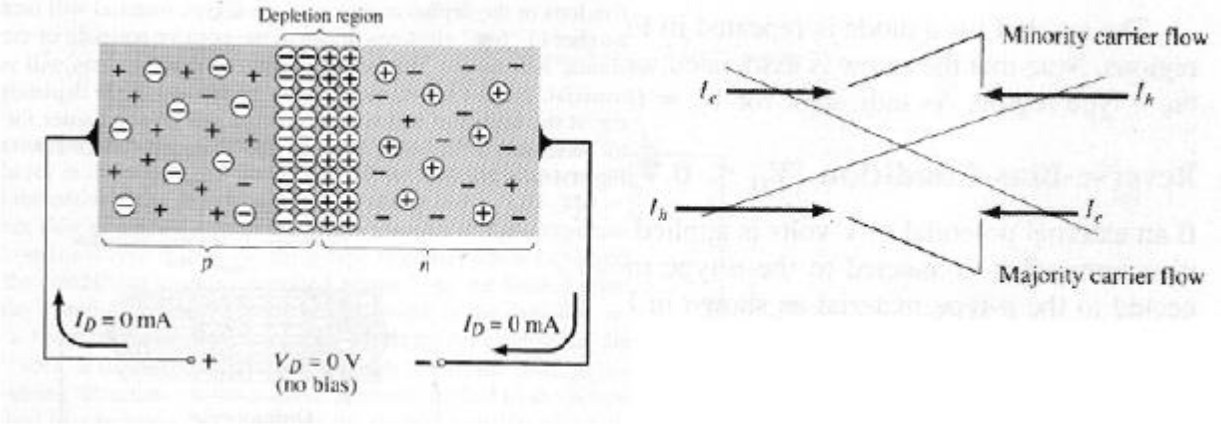
VD is the applied forward-bias voltage across the diode

where *k* is Boltzmann's constant =1.38 x 10^{-23} J/K

T_K is the absolute temperature in kelvins=273+the temperature in °C

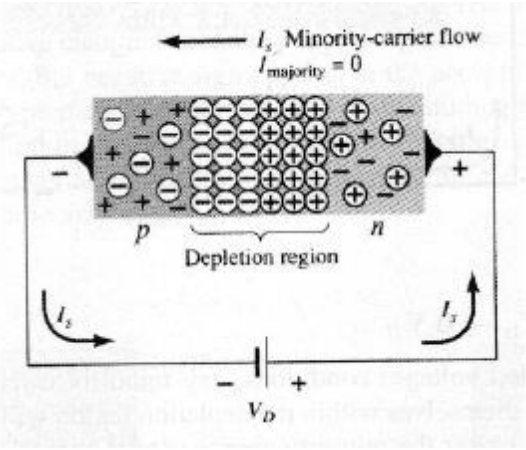
1-No Applied Bias (V_D =0 V)

In the absence of an applied bias voltage, the net flow of charge in any one direction for a semiconductor diode is zero



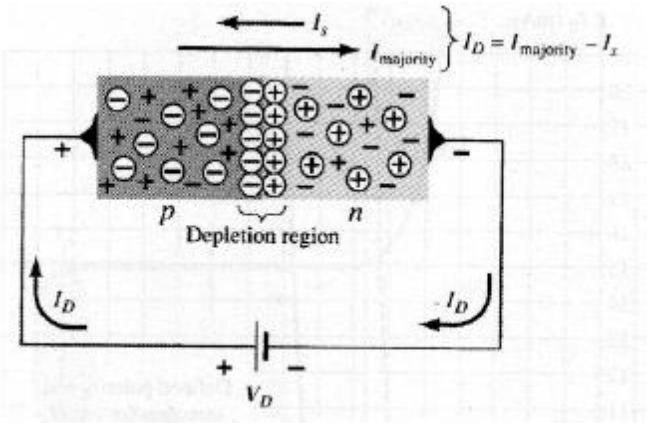
2-Reverse-Bias Condition ($V D < 0$ V)

The current that exists under reverse-bias conditions is called the reverse saturation current and is represented by *Is*



3-Forward-Bias Condition (*V D* > 0 V)

A semiconductor diode is forward-biased when the association p-type and positive and n-type and negative has been established

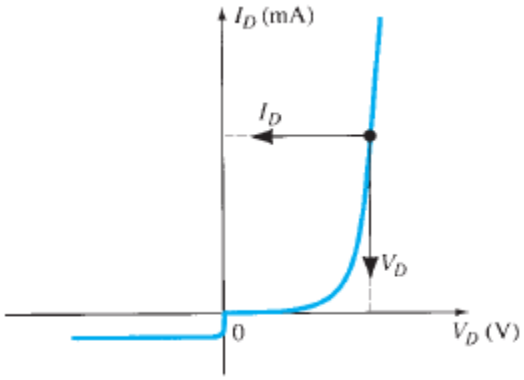


Resistance Levels

1. DC or Static Resistance:

The application of a dc voltage to a circuit containing a p-n junction diode will result in an operating point on the characteristic carve that will not change with time. The resistance of the diode at the operating point can found simply by finding the corresponding levels of V_D and I_D as shown in Fig. and applying the following equation:

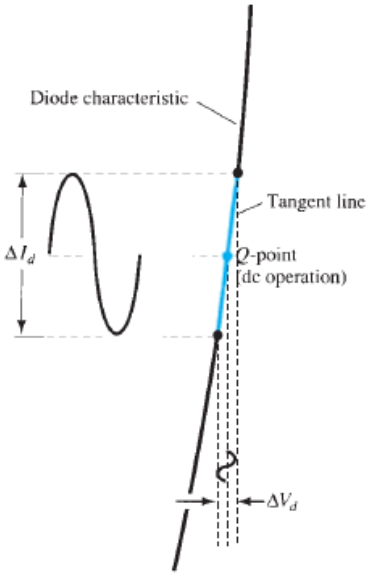
$$R_D = \frac{V_D}{I_D}$$

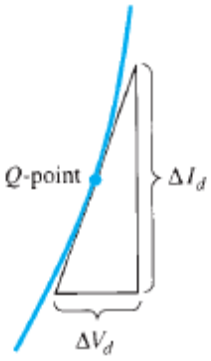


2. AC or Dynamic Resistance

If a sinusoidal rather than a dc input is applied, the situation will change completely. The varying input will move the instantaneous operating point up and down a region of the characteristics and thus defines a specific change in current and voltage as shown in Figure. With no applied varying signal, the point of operation would be the *Q* -point appearing on Figure, determined by the applied dc levels. The designation *Q-point* is derived from the word *quiescent,* which means "still or unvarying."

$$r_d = \frac{\Delta V_d}{\Delta I_d} \qquad r_d = \frac{26\text{ mV}}{I_D}$$

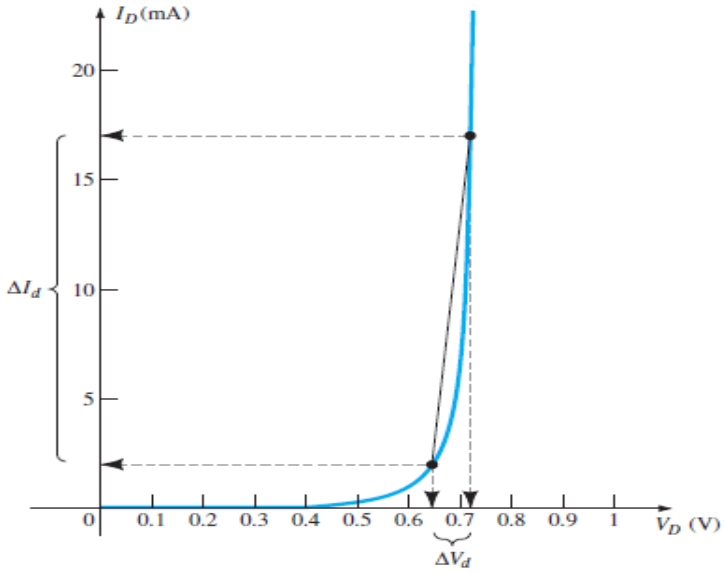




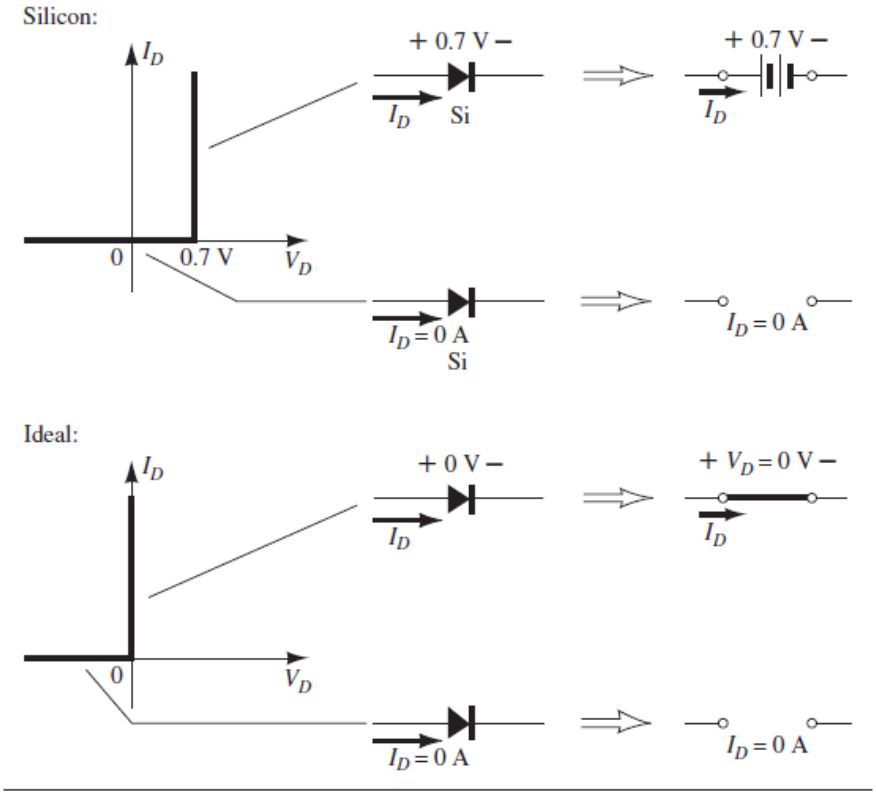
3. Average AC Resistance

If the input signal is sufficiently large to produce a broad swing such as indicated in Figure, the resistance associated with the device for this region is called the *average ac resistance.* The average ac resistance is, by definition, the resistance determined by a straight line drawn between the two intersections established by the maximum and minimum values of input voltage. In equation form

$$r_{av} = \left.\frac{\Delta V_d}{\Delta I_d}\right|_{\text{pt. to pt.}}$$



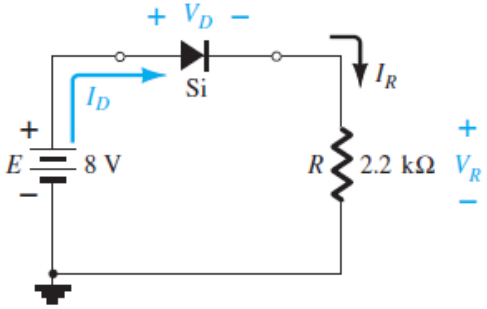
Approximate and Ideal Semiconductor Diode Models.



EXAMPLE 1:

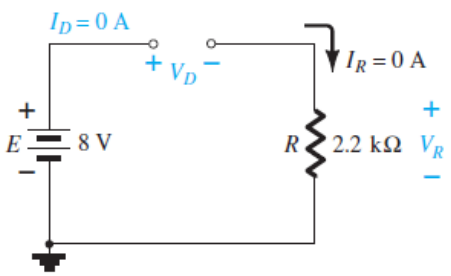
For the series diode configuration of Figure determine V_D, V_R, and I_D.

$$V_D = \mathbf{0.7\ V}$$
$$V_R = E - V_D = 8\ \text{V} - 0.7\ \text{V} = \mathbf{7.3\ V}$$
$$I_D = I_R = \frac{V_R}{R} = \frac{7.3\ \text{V}}{2.2\ \text{k}\Omega} \cong \mathbf{3.32\ mA}$$



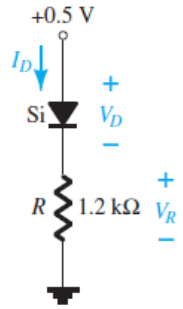
Repeat the Example with the diode reversed.

$$E - V_D - V_R = 0$$
$$V_D = E - V_R = E - 0 = E = 8\ \text{V}$$



EXAMPLE 2:

For the series diode configuration of Figure, determine V_D , V_R , and I_D .

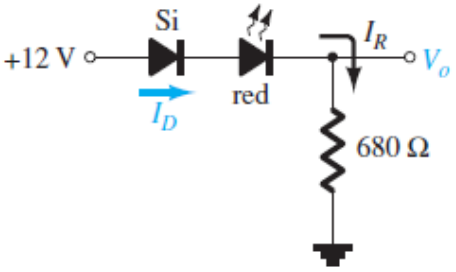


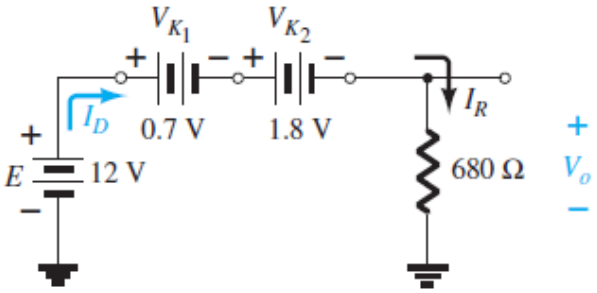
$$I_D = \mathbf{0\ A}$$
$$V_R = I_R R = I_D R = (0\ \text{A})1.2\ \text{k}\Omega = \mathbf{0\ V}$$
$$V_D = E = \mathbf{0.5\ V}$$

EXAMPLE 3:

Determine V_o and I_D for the series circuit of the figure.

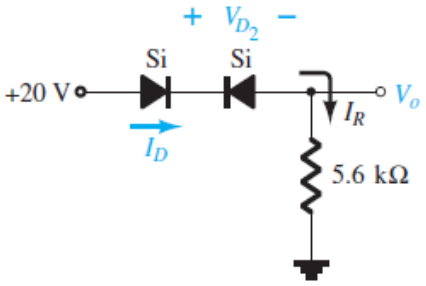
$$V_o = E - V_{K_1} - V_{K_2} = 12\ \text{V} - 2.5\ \text{V} = \mathbf{9.5\ V}$$
$$I_D = I_R = \frac{V_R}{R} = \frac{V_o}{R} = \frac{9.5\ \text{V}}{680\ \Omega} = \mathbf{13.97\ mA}$$





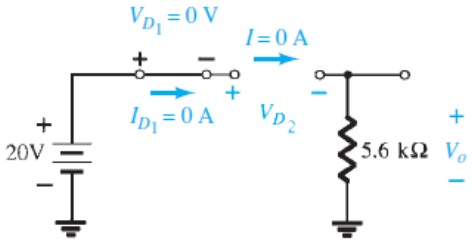
EXAMPLE 4:

Determine I_D , V_{D2}, and V_o for the circuit



$$V_o = I_R R = I_D R = (0\ \text{A})R = \mathbf{0\ V}$$
$$V_{D_2} = V_{\text{open circuit}} = E = \mathbf{20\ V}$$

$$E - V_{D_1} - V_{D_2} - V_o = 0$$
$$V_{D_2} = E - V_{D_1} - V_o = 20\ \text{V} - 0 - 0$$
$$= \mathbf{20\ V}$$
$$V_o = \mathbf{0\ V}$$

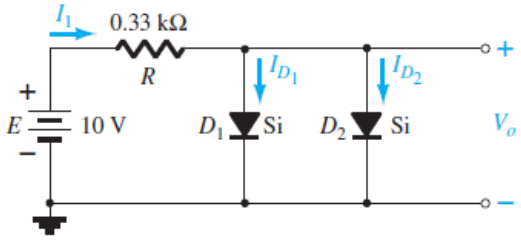


EXAMPLE 5:

Determine V_o, I_1, I_{D1}, and I_{D2} for the parallel diode configuration

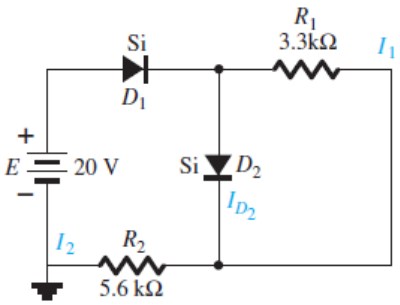
$$I_1 = \frac{V_R}{R} = \frac{E - V_D}{R} = \frac{10\text{ V} - 0.7\text{ V}}{0.33\text{ k}\Omega} = \mathbf{28.18\text{ mA}}$$

$$I_{D_1} = I_{D_2} = \frac{I_1}{2} = \frac{28.18\text{ mA}}{2} = \mathbf{14.09\text{ mA}}$$



H.W. :

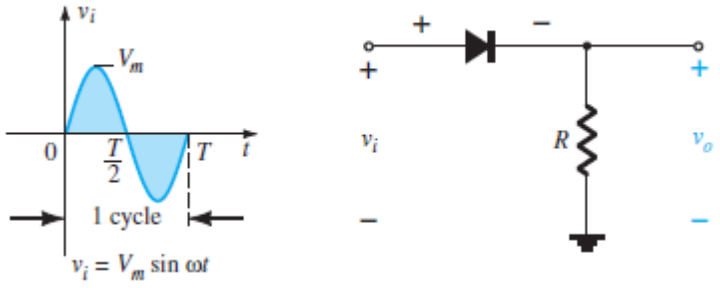
Determine the currents I_1 , I_2 , and I_{D2} for the network



SINUSOIDAL INPUTS:
1. HALF-WAVE RECTIFICATION

The diode analysis will now be expanded to include time-varying functions such as the sinusoidal waveform and the square wave. There is no question that the degree of difficulty will increase, but once a few fundamental maneuvers are understood, the analysis will be fairly direct and follow a common thread.

The simplest of networks to examine with a time-varying signal appears in figure. For the moment we will use the ideal model (note the absence of the Si, Ge, or GaAs label) to ensure that the approach is not clouded by additional mathematical complexity.



Over one full cycle, defined by the period *T* of figure, the average value (the algebraic sum of the areas above and below the axis) is zero. The circuit of above figure, called a ***half-wave rectifier***, will generate a waveform *v o* that will have an average value of particular use in the ac-to-dc conversion process. When employed in the rectification process, a diode is typically referred to as a ***rectifier***.

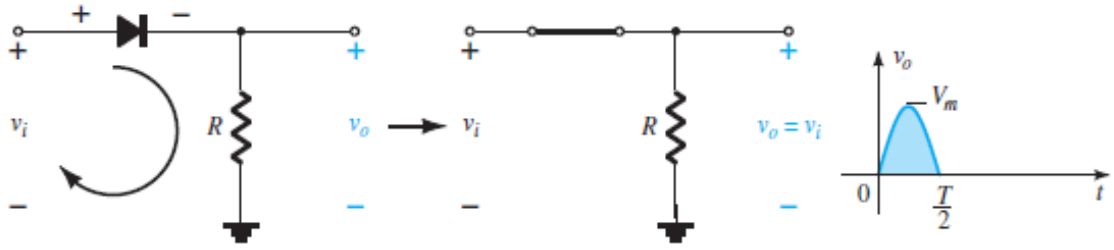
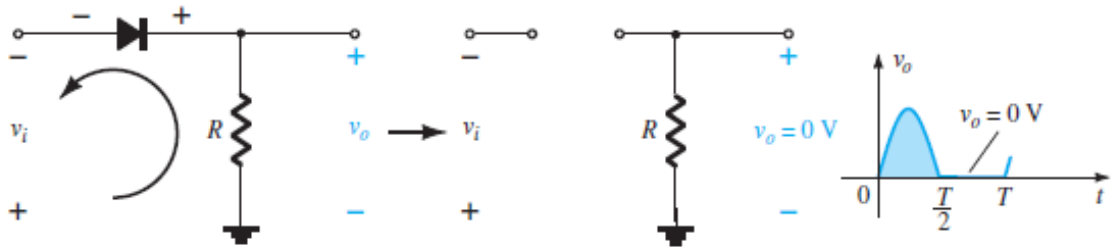
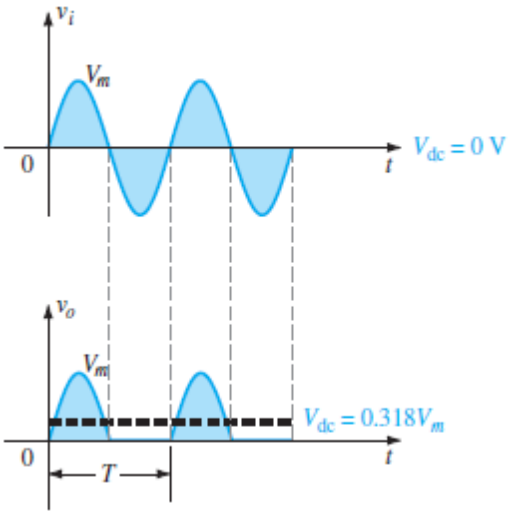


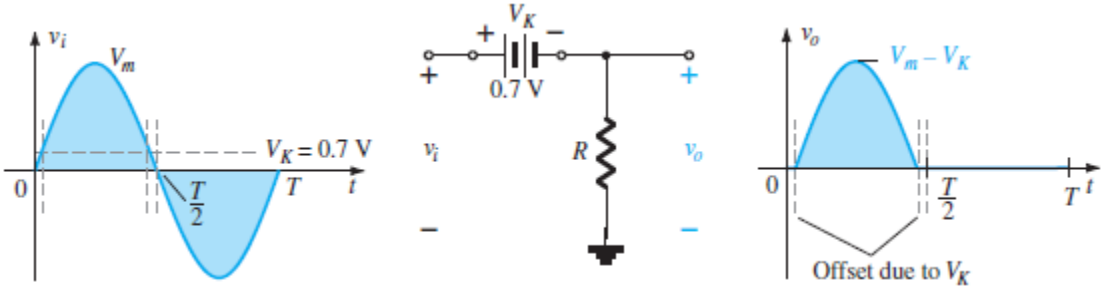
FIG. 2.45
Conduction region (0 → T/2).





$V_{dc} = 0.318\,V_m$ half-wave if V_m is sufficiently greater than V_K

The effect of using a silicon diode with V_K = 0.7 V is demonstrated in Fig. below for the forward-bias region. The applied signal must now be at least 0.7 V before the diode can turn "on." For levels of v_i less than 0.7V, the diode is still in an open-circuit state and v_o=0 V, as shown in the same figure. When conducting, the difference between v_o and v_i is a fixed



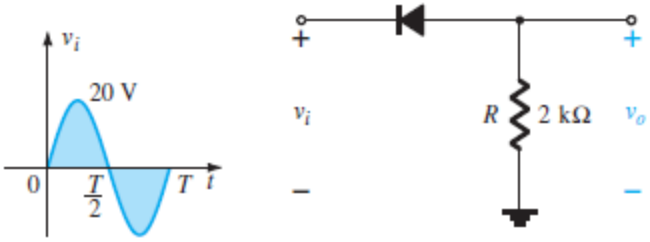
level of V_K=0.7 V and $V_o = V_i - V_K$, as shown in the figure. The net effect is a reduction in area above the axis, which reduces the resulting dc voltage level. For situations where $V_m >> V_K$, the following equation can be applied to determine the average value with a relatively high level of accuracy.

$$V_{dc} \cong 0.318(V_m - V_K)$$

In fact, if V_m is sufficiently greater than V_K, is often applied as a first approximation for V_{dc}.

EXAMPLE 6

a. Sketch the output *v o* and determine the dc level of the output for the network of the figure.
b. Repeat part (a) if the ideal diode is replaced by a silicon diode.

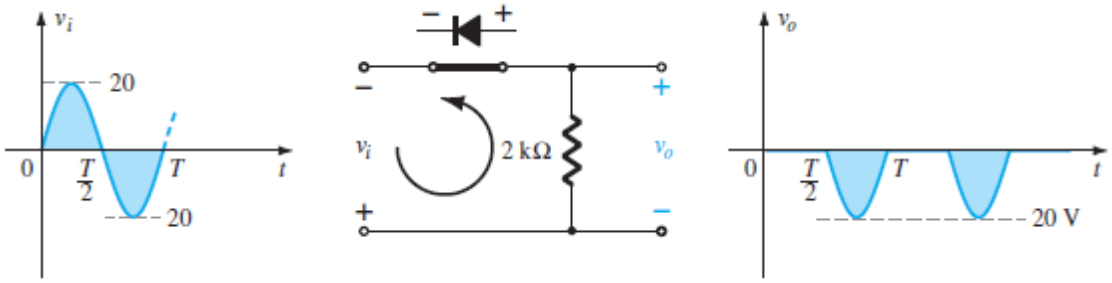


Solution:

a. In this situation the diode will conduct during the negative part of the input as shown in figure below, and v_o will appear as shown in the same figure. For the full period, the dc level is

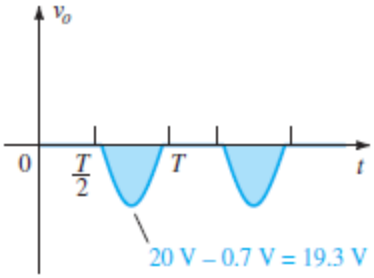
$$V_{dc} = -0.318V_m = -0.318(20\text{ V}) = \mathbf{-6.36\text{ V}}$$

The negative sign indicates that the polarity of the output is opposite to the defined polarity.



b. For a silicon diode, the output has the appearance of the figure below.

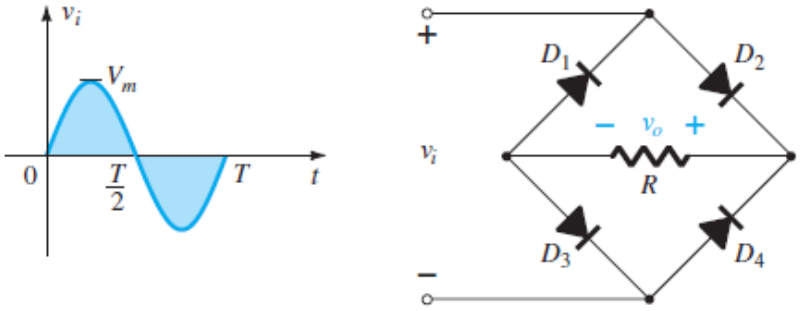
$$V_{dc} \cong -0.318(V_m - 0.7\text{ V}) = -0.318(19.3\text{ V}) \cong \mathbf{-6.14\text{ V}}$$



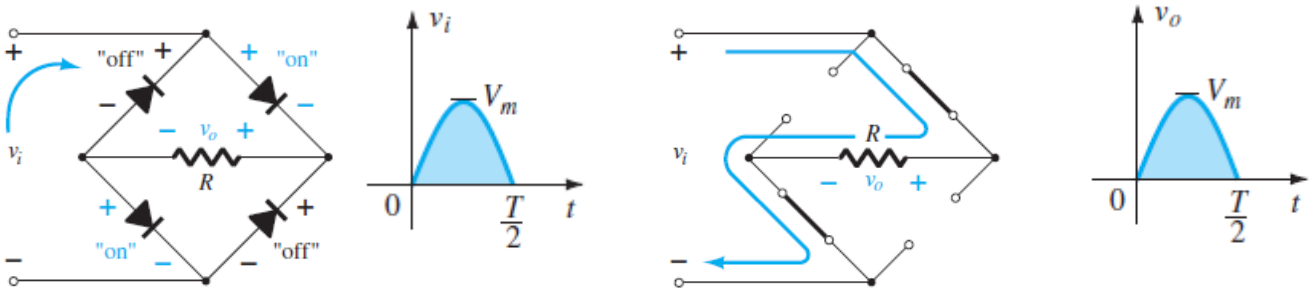
2.FULL -WAVE RECTIFICATION

A-Bridge Network:

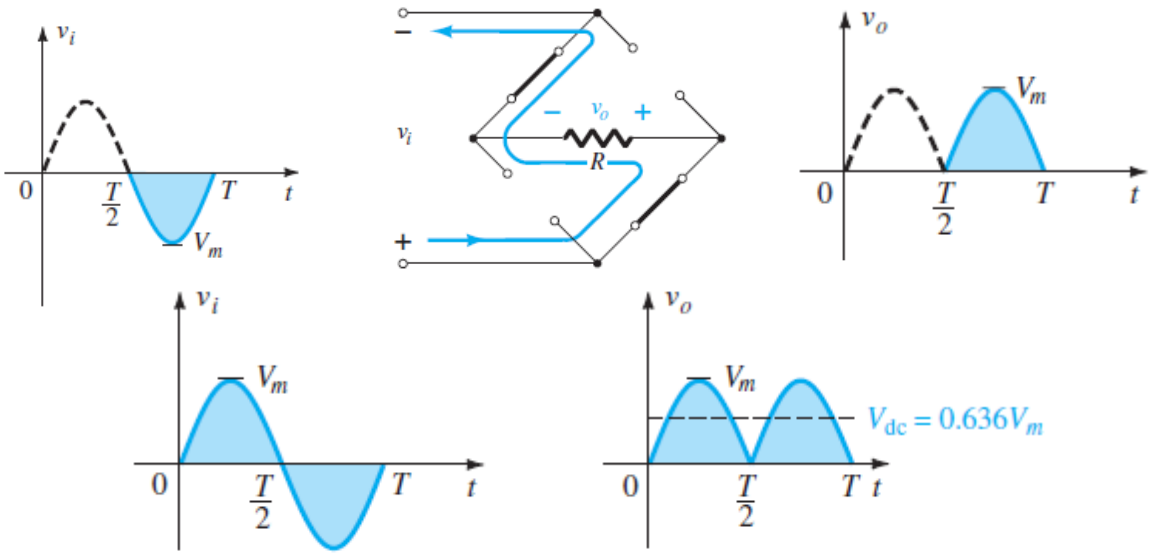
The dc level obtained from a sinusoidal input can be improved 100% using a process called ***full-wave rectification***



The resulting polarities across the ideal diodes are also shown in figure to reveal that *D*2 and *D*3 are conducting, whereas *D*1 and *D*4 are in the "off" state.



For the negative region of the input the conducting diodes are *D*1 and *D*4, resulting in the configuration of figure below.



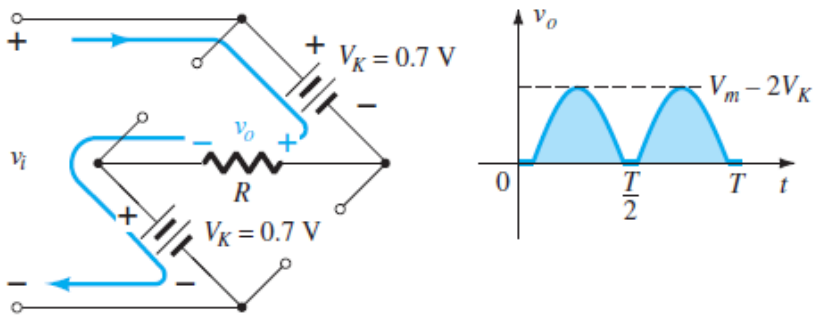
Since the area above the axis for one full cycle is now twice that obtained for a half-wave system, the dc level has also been doubled and

$$V_{dc} = 2(0.318Vm)$$

$$\boxed{V_{dc} = 0.636\,V_m} \quad \text{full-wave}$$

If silicon rather than ideal diodes is employed as shown in figure below, the application of Kirchhoff's voltage law around the conduction path results in

$$vi - V_K - vo - V_K = 0$$
$$vo = vi - 2V_K$$



The peak value of the output voltage *vo* is therefore

$$Vo_{max} = V_m - 2V_K$$

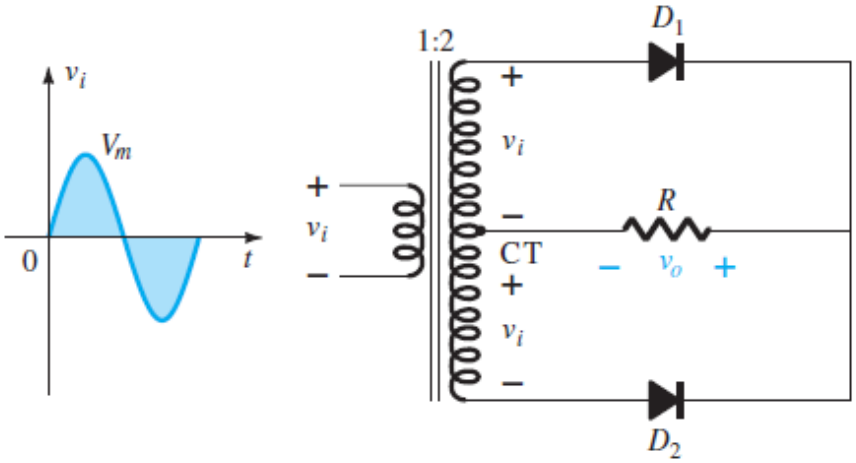
For situations where $V_m >> 2V_K$, the following equation can be applied for the average value with a relatively high level of accuracy:

$$\boxed{V_{dc} \cong 0.636(V_m - 2V_K)}$$

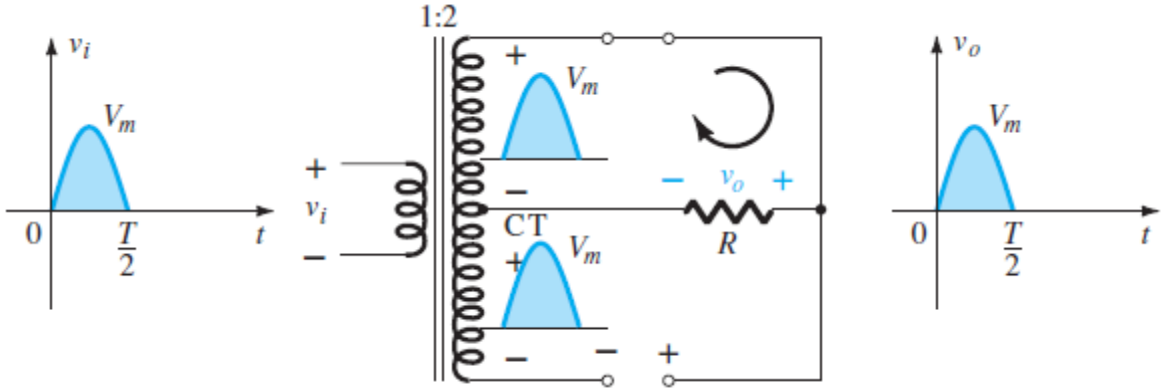
Then again, if V_m is sufficiently greater than $2V_K$, then Equation $\boxed{V_{dc} = 0.636\,V_m}$ is often applied as a first approximation for V_{dc}.

B-Center-Tapped Transformer

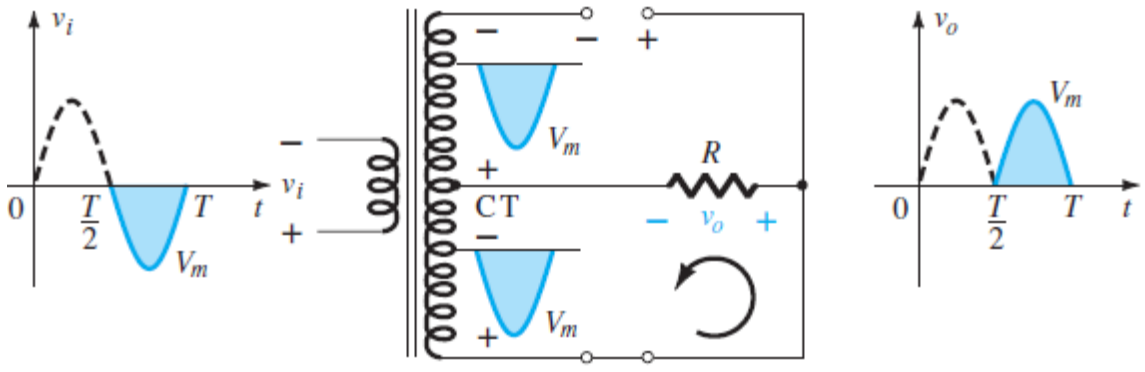
A second popular full-wave rectifier appears in figure with only two diodes but requiring a center-tapped (CT) transformer to establish the input signal across each section of the secondary of the transformer.



During the positive portion of *vi* applied to the primary of the transformer, the network will appear as shown in figure below with a positive pulse across each section of the secondary coil. *D*1 assumes the short-circuit equivalent and *D*2 the open-circuit equivalent.



During the negative portion of the input the network appears as shown in figure, reversing the roles of the diodes but maintaining the same polarity for the voltage across the load resistor *R*. The net effect is the same output as that appearing in figure with the same dc levels.



Clippers and Clampers

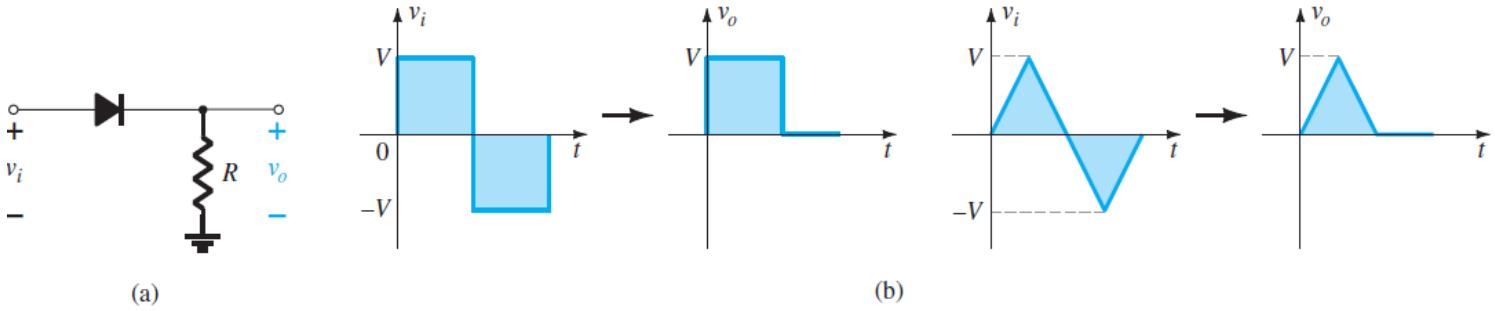
The previous section on rectification gives clear evidence that diodes can be used to change the appearance of an applied waveform. This section on clippers and the next on clampers will expand on the wave-shaping abilities of diodes.

Clippers are networks that employ diodes to "clip" away a portion of an input signal without distorting the remaining part of the applied waveform

There are two general categories of clippers: ***series*** and ***parallel***. The series configuration is defined as one where the diode is in series with the load, whereas the parallel variety has the diode in a branch parallel to the load.

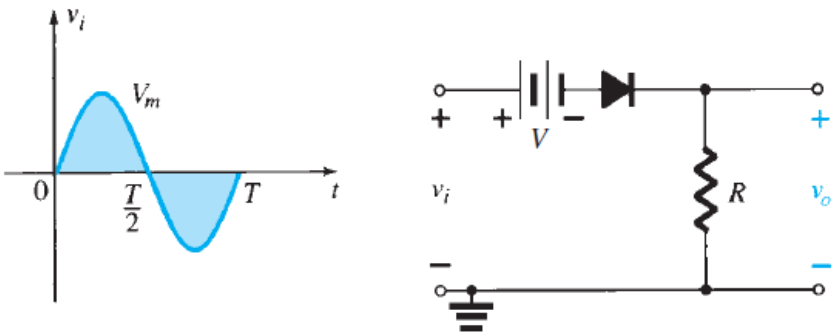
A. Series

The response of the series configuration in figure (a) to a variety of alternating waveforms is provided in figure (b) below. Although first introduced as a half-wave rectifier (for sinusoidal waveforms), there are no boundaries on the type of signals that can be applied to a clipper.



(a) (b)

The addition of a dc supply to the network as shown in figure below can have a pronounced effect on the analysis of the series clipper configuration. The response is not as obvious because the dc supply can aid or work against the source voltage, and the dc supply can be in the leg between the supply and output or in the branch parallel to the output.



There are some things one can do to give the analysis some direction. First and most important:

1.Take careful note of where the output voltage is defined.

2.Try to develop an overall sense of the response by simply noting the "pressure" established by each supply and the effect it will have on the conventional current direction through the diode.

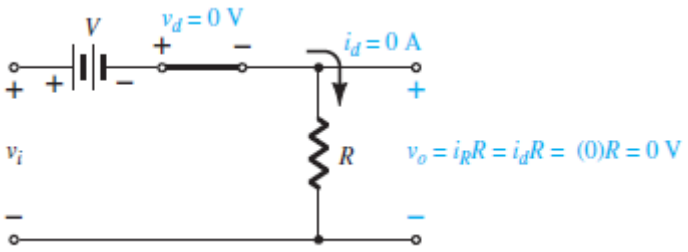
In previous figure, for instance, any positive voltage of the supply will try to turn the diode on by establishing a conventional current through the diode that matches the arrow in the diode symbol. However, the added dc supply *V* will oppose that applied voltage and try to keep the diode in the "off" state. The result is that any supply voltage greater than *V* volts will turn the diode on and conduction can be established through the load resistor. Keep in mind that we are dealing with an ideal diode for the moment, so the turn-on voltage is simply 0 V. In general, we can conclude that the diode will be on for any voltage *vi* that is greater than *V* volts and off for any lesser voltage. For the "off" condition, the output would be 0 V due to the lack of current, and for the "on" condition it would simply be $v_o = v_i - V$ as determined by Kirchhoff's voltage law.

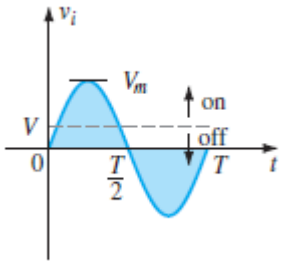
3. Determine the applied voltage (transition voltage) that will result in a change of state for the diode from the "off" to the "on" state.

This step will help to define a region of the applied voltage when the diode is on and when it is off. On the characteristics of an ideal diode this will occur when V_D=0 V and I_D=0 mA. For the approximate equivalent this is determined by finding the applied voltage when the diode has a drop of 0.7 V across it (for silicon) and I_D=0 mA. Note the substitution of the short-circuit equivalent for the diode and the fact that the voltage across the resistor is 0 V because the diode current is 0 mA. The result is $v_i - V = 0$, and so

$$v_i = V$$

is the transition voltage.



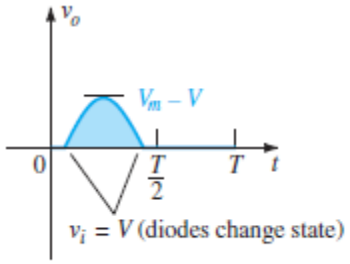


$$v_o = v_i - V$$

4. It is often helpful to draw the output waveform directly below the applied voltage using the same scales for the horizontal axis and the vertical axis.

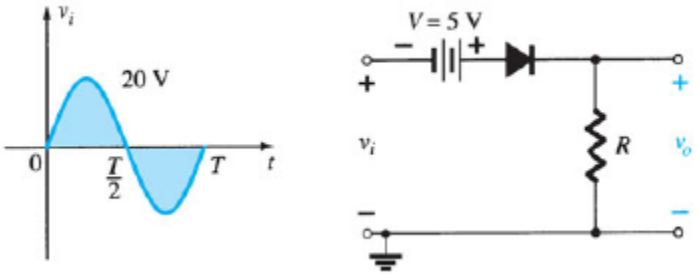
Using this last piece of information, we can establish the 0-V level on the plot of figure below for the region indicated. For the "on" condition, the above equation can be used to find the output voltage when the applied voltage has its peak value:

$$v_{o\,\text{peak}} = V_m - V$$



EXAMPLE 7

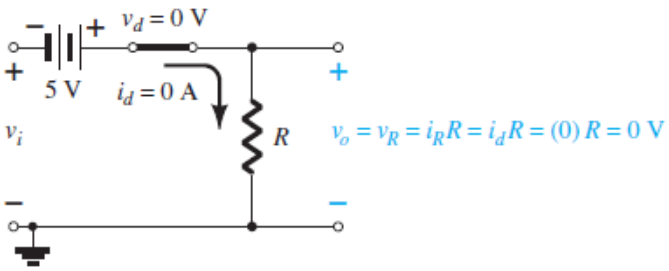
Determine the output waveform for the sinusoidal input



The transition model is substituted in figure below, and we find that the transition from one state to the other will occur when

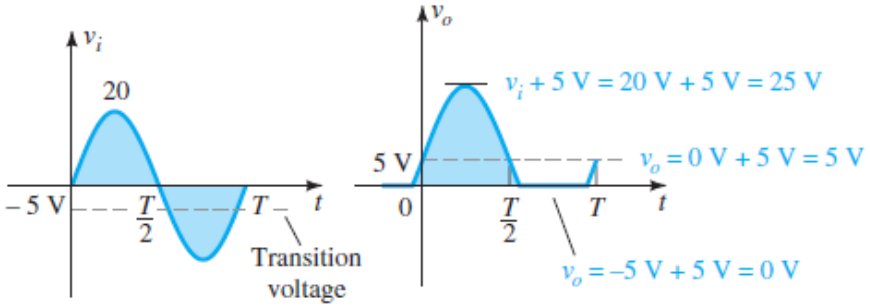
$$vi + 5\ V = 0\ V$$

or $$vi = -5\ V$$



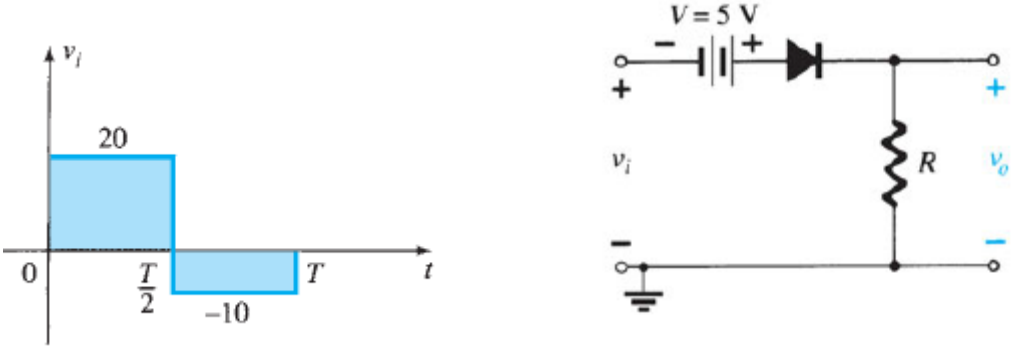
In figure below a horizontal line is drawn through the applied voltage at the transition level. For voltages less than -5V the diode is in the open-circuit state and the output is 0V, as shown in the sketch of *vo*. Using figure below, we find that for conditions when the diode is on and the diode current is established the output voltage will be the following, as determined using Kirchhoff's voltage law:

$$vo = vi + 5\ V$$



EXAMPLE 8

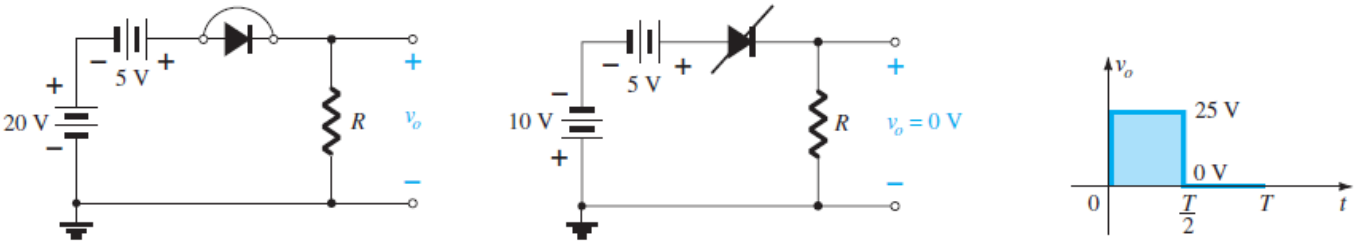
Find the output voltage for the network examined in the figure



Solution:

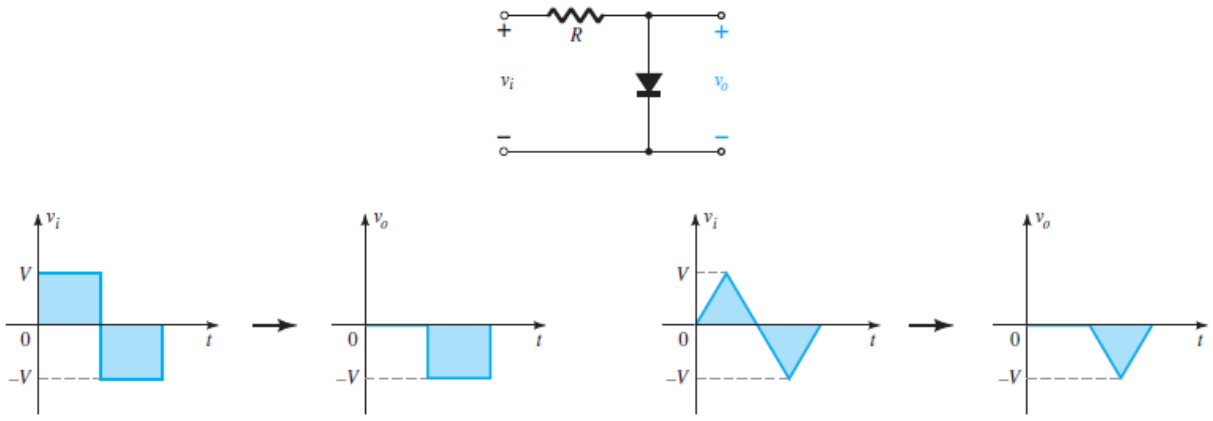
For *vi* = 20 V (0 *T*/2) the network of Fig. 2.78 results. The diode is in the short-circuit state, and *vo* = 20 V + 5 V = 25 V. For *vi* = -10 V the network

results, placing the diode in the "off" state, and $vo = i_R R = (0)R = 0$ V.



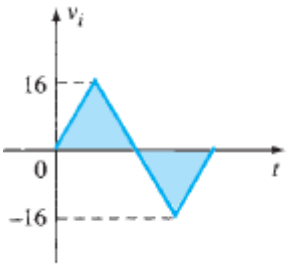
B. Parallel

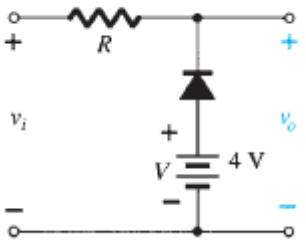
The network of figure below is the simplest of parallel diode configurations with the output. The analysis of parallel configurations is very similar to that applied to series configurations, as demonstrated in the next example.



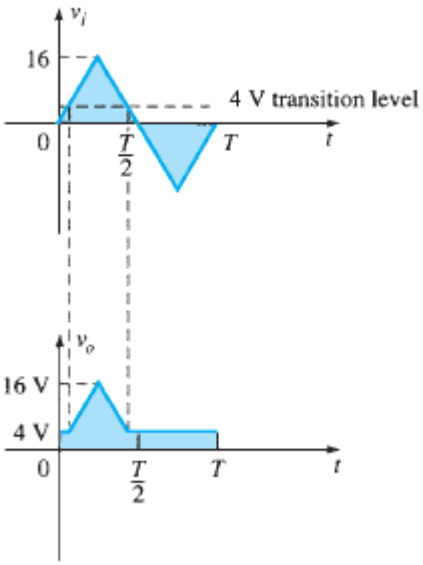
EXAMPLE 9

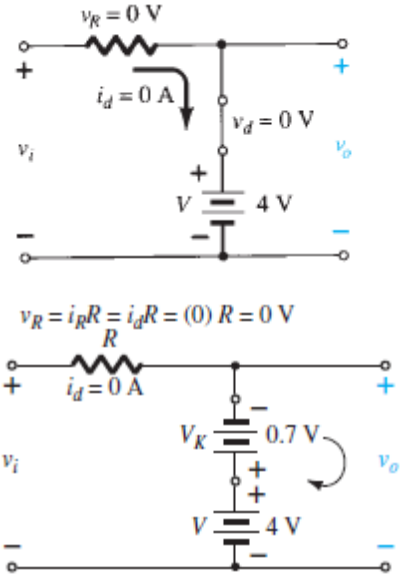
Determine *vo* for the network





Solution:





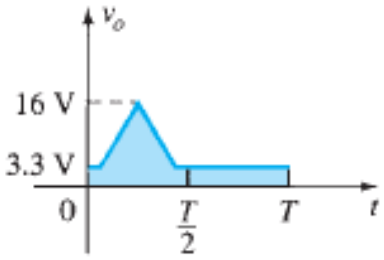
If the diode is silicon:

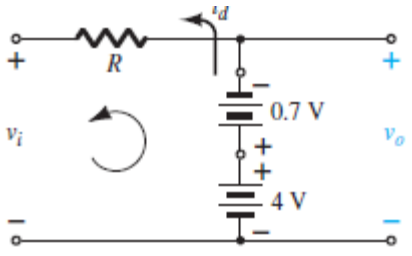
$$vi + V_K - V = 0$$

and $$vi = V - V_K = 4\text{V} - 0.7\text{ V} = \mathbf{3.3\ V}$$

For input voltages greater than 3.3 V, the diode will be an open circuit and *vo* = *vi*. For input voltages less than 3.3 V, the diode will be in the "on" state

$$vo = 4\text{ V} - 0.7\text{V} = \mathbf{3.3\ V}$$

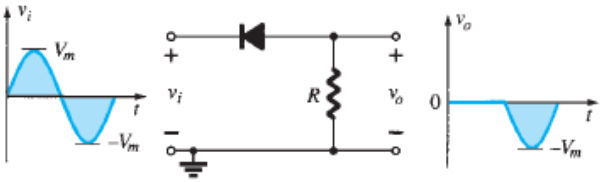




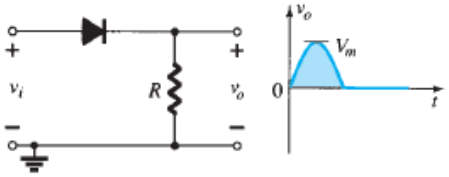
Summary (مهم جدا)

Simple Series Clippers (Ideal Diodes)

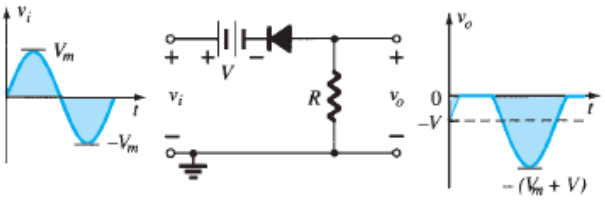
POSITIVE

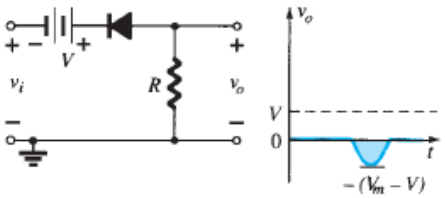


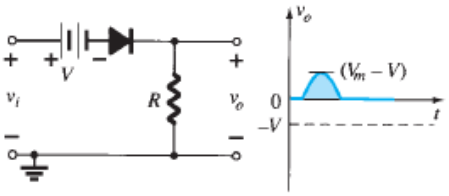
NEGATIVE

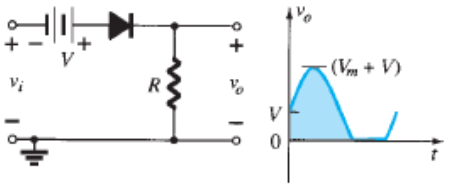


Biased Series Clippers (Ideal Diodes)

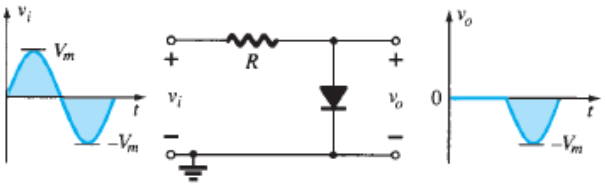


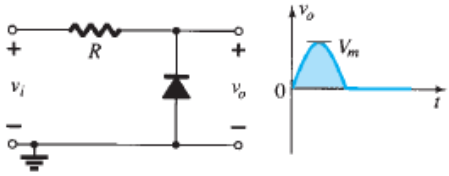




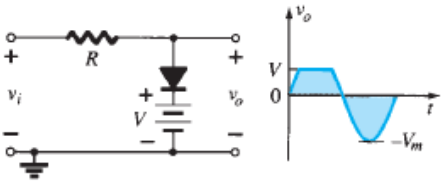


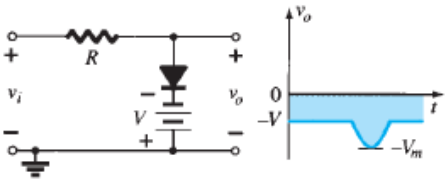
Simple Parallel Clippers (Ideal Diodes)

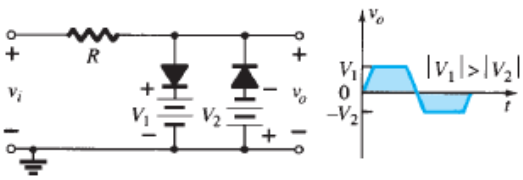


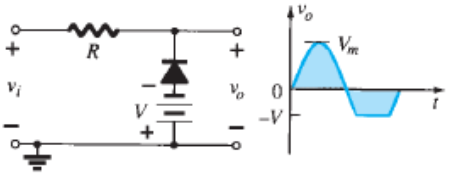


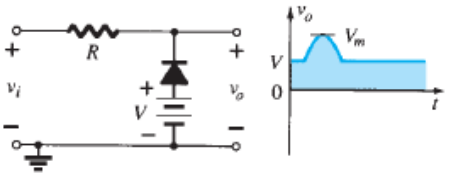
Biased Parallel Clippers (Ideal Diodes)









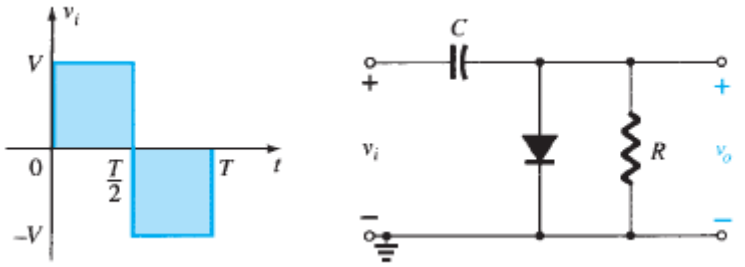


Clampers

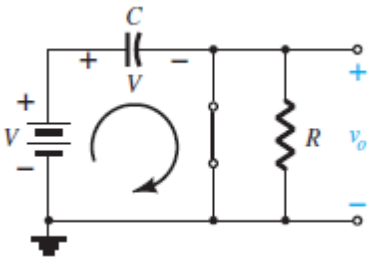
A clamper is a network constructed of a diode, a resistor, and a capacitor that shifts a waveform to a different dc level without changing the appearance of the applied signal.

Additional shifts can also be obtained by introducing a dc supply to the basic structure. The chosen resistor and capacitor of the network must be chosen such that the time constant determined by $\tau = RC$ is sufficiently large to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is nonconducting. Throughout the analysis we assume that for all practical purposes the capacitor fully charges or discharges in five time constants.

Clamping networks have a capacitor connected directly from input to output with a resistive element in parallel with the output signal. The diode is also in parallel with the output signal but may or may not have a series dc supply as an added element.



For the interval 0 to *T*/2 the network will appear as shown in Fig. below. The short-circuit equivalent for the diode will result in *vo*= 0V for this time interval. During this same interval of time, the time constant determined by τ=RC is very small because the resistor R has been effectively "shorted out" by the conducting diode. The result is that the capacitor will quickly charge to the peak value of V volts

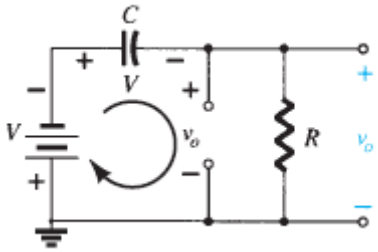


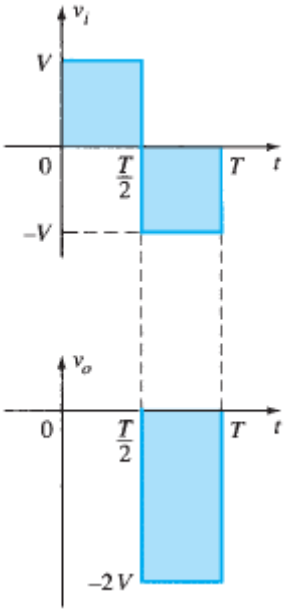
When the input switches to the -*V* state, the network will appear as shown in Fig. below, with the open-circuit equivalent for the diode determined by the applied signal and stored voltage across the capacitor—both "pressuring" current through the diode from cathode to anode. Now that *R* is

back in the network the time constant determined by the *RC* product is sufficiently large to establish a discharge period 5τ, much greater than the period $T/2 \rightarrow T$, Applying Kirchhoff's voltage law around the input loop results in

$$-V - V - vo = 0$$

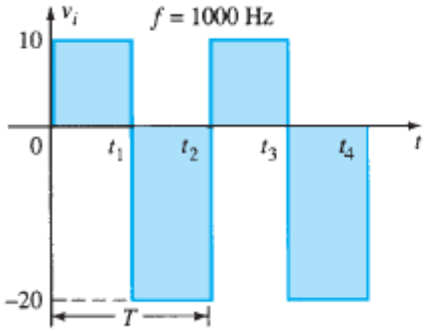
$$vo = -2V$$

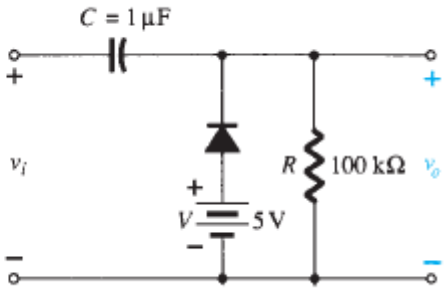




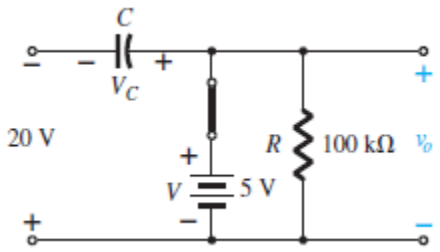
EXAMPLE 10

Determine *v o* for the network





Solution: The analysis of clamping circuits is started by considering that the part of the input signal that will forward bias the diode. For the circuit, the diode is forward bias ("on" state) during the negative half period of the input signal (*vi*) and the capacitor will charge up instantaneously to a voltage level determined by the circuit.



For the input section KVL will result in

$$-20\text{ V} + VC - 5\text{ V} = 0$$

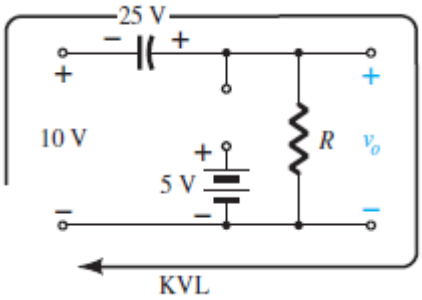
$$VC = 25\text{ V}$$

The capacitor will therefore charge up to 25 V. In this case the resistor *R* is not shorted out by the diode.

The open-circuit equivalent for the diode removes the 5-V battery from having any effect on *vo*, and applying Kirchhoff's voltage law around the outside loop of the network results in

$$+10\text{ V} + 25\text{ V} - vo = 0$$

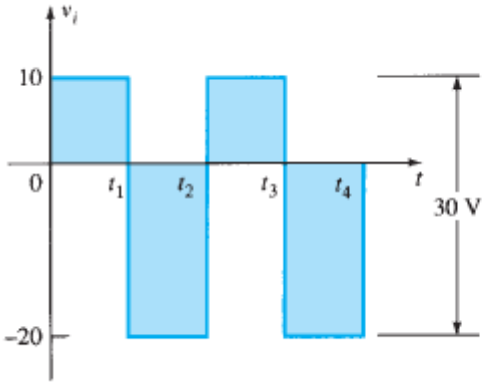
$$vo = 35\text{ V}$$

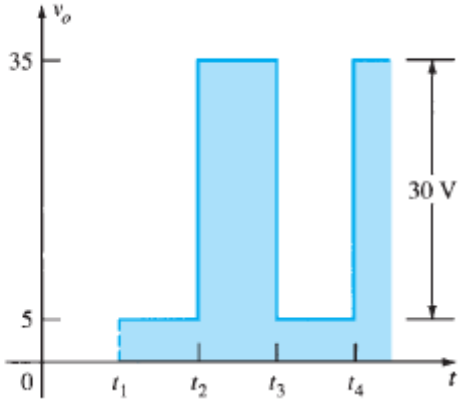


The time constant of the discharging network of above figure is determined by the product *RC* and has the magnitude $\tau = RC = (100\text{ k}\Omega)(0.1\ \mu\text{F}) = 0.01\text{ s} = 10\text{ ms}$

The total discharge time is therefore $5\tau = 5(10\text{ ms}) = 50\text{ ms}$.

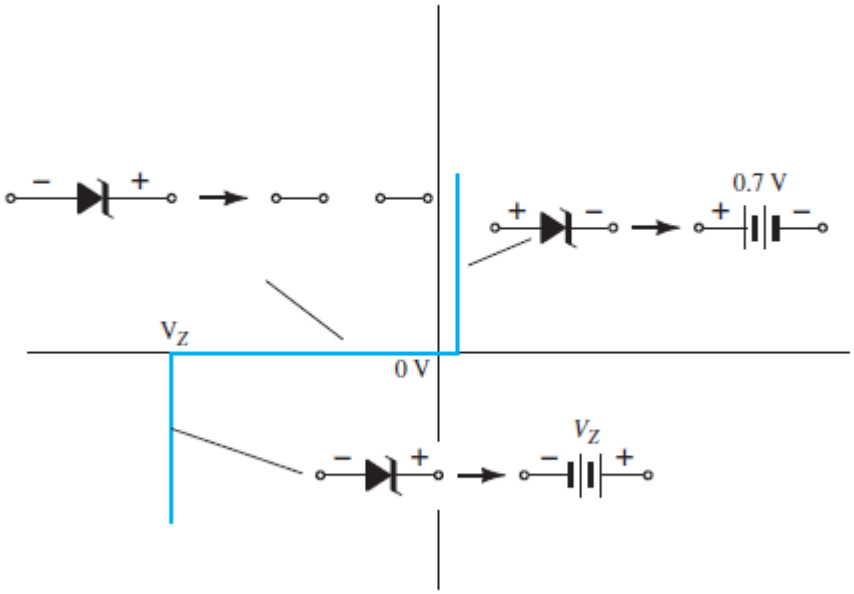
Since the interval $t_2 \rightarrow t_3$ will only last for 0.5 ms, it is certainly a good approximation that the capacitor will hold its voltage during the discharge period between pulses of the input signal. The resulting output appears in Fig. below with the input signal. Note that the output swing of 30 V matches the input swing.





ZENER DIODES

The analysis of networks employing Zener diodes is quite similar to the analysis of semiconductor Diodes First the state of the diode must be determined, followed by a substitution of the appropriate model and a determination of the other unknown quantities of the network. Figure below reviews the approximate equivalent circuits for each region of a Zener diode assuming the straight-line approximations at each break point. Note that the forward-bias region is included because occasionally an application will skip into this region also. The use of a Zener diode as a *regulator* will then be described in detail because it is one of its major areas of application. A regulator is a combination of elements designed to ensure that the output voltage of a supply remains fairly constant.

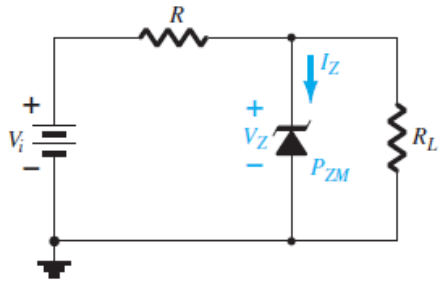


The use of the Zener diode as a regulator is so common that three conditions surrounding the analysis of the basic Zener regulator are considered.

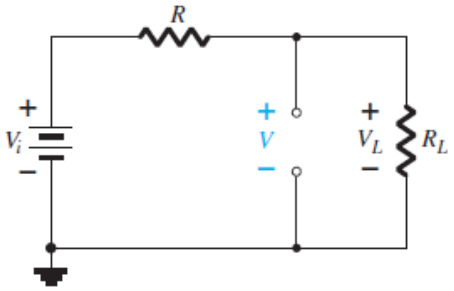
1- **V_i and R_L Fixed**
2- **Fixed V_i, Variable R_L**
3- **Fixed R_L, Variable V_i**

1.V_i and R_L fixed

The simplest of Zener diode regulator networks appears in Fig. below. The applied dc voltage is fixed, as is the load resistor. The analysis can fundamentally be broken down into two steps.



1. ***Determine the state of the Zener diode by removing it from the network and calculating the voltage across the resulting open circuit.***



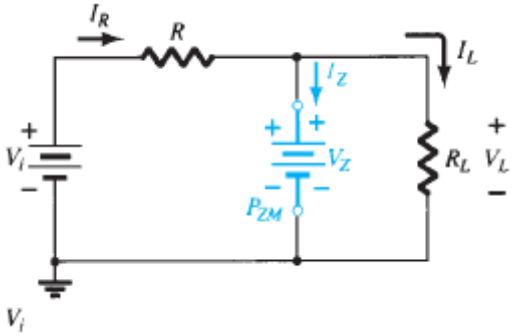
$$V = V_L = \frac{R_L V_i}{R + R_L}$$

If $V \geq V_Z$, the Zener **diode is on**, and the appropriate equivalent model can be substituted.

If $V < V_Z$, the **diode is off**, and the open-circuit equivalence is substituted.

2. ***Substitute the appropriate equivalent circuit and solve for the desired unknowns.***

$$V_L = V_Z$$



$$I_R = I_Z + I_L$$

$$\boxed{I_Z = I_R - I_L}$$

where

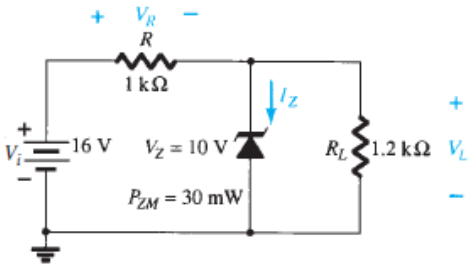
$$I_L = \frac{V_L}{R_L} \quad \text{and} \quad I_R = \frac{V_R}{R} = \frac{V_i - V_L}{R}$$

The power dissipated by the Zener diode is determined by

$$\boxed{P_Z = V_Z I_Z}$$

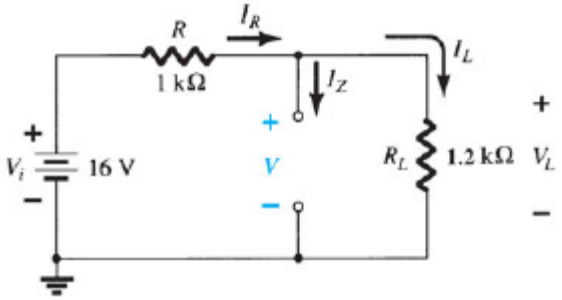
EXAMPLE 11

For the Zener diode network, determine V_L , V_R, I_Z, and P_Z



Solution:

$$V = \frac{R_L V_i}{R + R_L} = \frac{1.2\,\text{k}\Omega(16\,\text{V})}{1\,\text{k}\Omega + 1.2\,\text{k}\Omega} = 8.73\,\text{V}$$

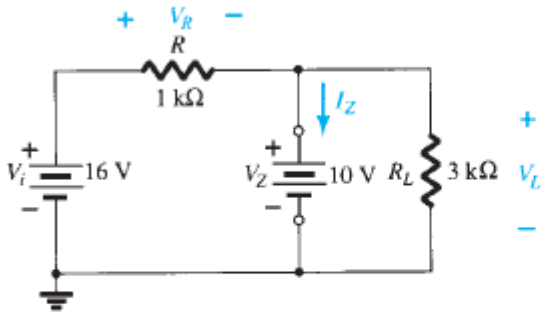


$$V_L = V = \mathbf{8.73\,V}$$
$$V_R = V_i - V_L = 16\,\text{V} - 8.73\,\text{V} = \mathbf{7.27\,V}$$
$$I_Z = \mathbf{0\,A}$$
$$P_Z = V_Z I_Z = V_Z(0\,\text{A}) = \mathbf{0\,W}$$

If $R_L = 3\ \text{k}\Omega$

$$V = \frac{R_L V_i}{R + R_L} = \frac{3\ \text{k}\Omega(16\ \text{V})}{1\ \text{k}\Omega + 3\ \text{k}\Omega} = 12\ \text{V}$$

$$V_L = V_Z = \mathbf{10\ V}$$
$$V_R = V_i - V_L = 16\ \text{V} - 10\ \text{V} = \mathbf{6\ V}$$
$$I_L = \frac{V_L}{R_L} = \frac{10\ \text{V}}{3\ \text{k}\Omega} = 3.33\ \text{mA}$$
$$I_R = \frac{V_R}{R} = \frac{6\ \text{V}}{1\ \text{k}\Omega} = 6\ \text{mA}$$
$$I_Z = I_R - I_L\ [\text{Eq. (2.18)}]$$
$$= 6\ \text{mA} - 3.33\ \text{mA}$$
$$= \mathbf{2.67\ mA}$$



The power dissipated is

$$P_Z = V_Z I_Z = (10\ \text{V})(2.67\ \text{mA}) = \mathbf{26.7\ mW}$$

which is less than the specified $P_{ZM} = 30\ \text{mW}$.

2. Fixed V_i, Variable R_L

Due to the offset voltage V_Z, there is a specific range of resistor values (and therefore load current) that will ensure that the Zener is in the "on" state. Too small a load resistance R_L will result in a voltage V_L across the load resistor less than V_Z, and the Zener device will be in the "off" state.
To determine the minimum load resistance that will turn the Zener diode on, simply calculate the value of R_L that will result in a load voltage $V_L=V_Z$. That is,

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

Solving for R_L, we have

$$\boxed{R_{L_{\min}} = \frac{RV_Z}{V_i - V_Z}}$$

Any load resistance value greater than the R_L obtained from the above equation will ensure that the Zener diode is in the "on" state and the diode can be replaced by its V_Z source equivalent. The condition defined by the above equation establishes the minimum R_L, but in turn specifies the maximum I_L as

$$\boxed{I_{L_{\max}} = \frac{V_L}{R_L} = \frac{V_Z}{R_{L_{\min}}}}$$

Once the diode is in the "on" state, the voltage across R remains fixed at

$$V_R = V_i - V_Z$$

and I_R remains fixed at

$$I_R = \frac{V_R}{R}$$

The Zener current

$$I_Z = I_R - I_L$$

resulting in a minimum I_Z when I_L is a maximum and a maximum I_Z when I_L is a minimum value, since I_R is constant.

Since I_Z is limited to I_{ZM} as provided on the data sheet, it does affect the range of R_L and therefore I_L. Substituting I_{ZM} for I_Z establishes the minimum I_L as

$$I_{L_{min}} = I_R - I_{ZM}$$

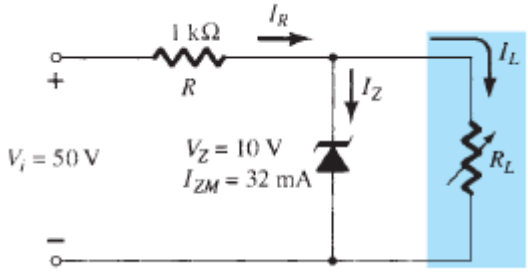
and the maximum load resistance as

$$R_{L_{max}} = \frac{V_Z}{I_{L_{min}}}$$

EXAMPLE 12

a. For the network, determine the range of R_L and I_L that will result in V_{RL} being maintained at 10V.

b. Determine the maximum wattage rating of the diode.



Solution:

a. To determine the value of R_L that will turn the Zener diode on, apply Eq. (2.20):

$$R_{L_{min}} = \frac{RV_Z}{V_i - V_Z} = \frac{(1\,\text{k}\Omega)(10\,\text{V})}{50\,\text{V} - 10\,\text{V}} = \frac{10\,\text{k}\Omega}{40} = \mathbf{250\ \Omega}$$

The voltage across the resistor R is then determined by Eq. (2.22):

$$V_R = V_i - V_Z = 50\,\text{V} - 10\,\text{V} = \mathbf{40\ V}$$

and Eq. (2.23) provides the magnitude of I_R:

$$I_R = \frac{V_R}{R} = \frac{40\,\text{V}}{1\,\text{k}\Omega} = \mathbf{40\ mA}$$

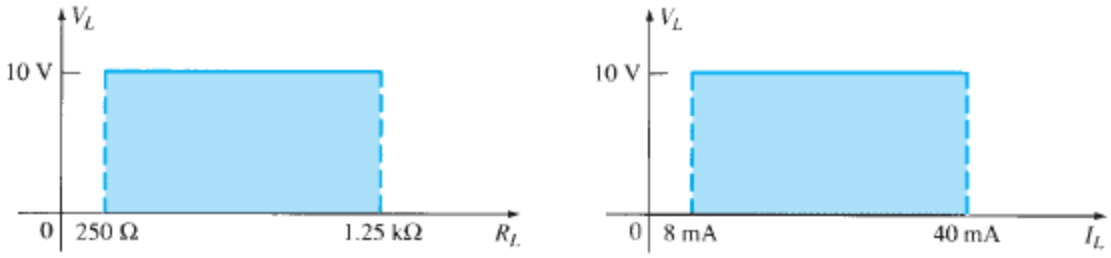
The minimum level of I_L is then determined by Eq. (2.25):

$$I_{L_{min}} = I_R - I_{ZM} = 40\,\text{mA} - 32\,\text{mA} = \mathbf{8\ mA}$$

with Eq. (2.26) determining the maximum value of R_L:

$$R_{L_{max}} = \frac{V_Z}{I_{L_{min}}} = \frac{10\,\text{V}}{8\,\text{mA}} = \mathbf{1.25\ k\Omega}$$

A plot of V_L versus R_L appears in Fig. 2.120a and for V_L versus I_L in Fig. 2.120b.



(a) (b)

b. $P_{max} = V_Z I_{ZM}$
$= (10\,\text{V})(32\,\text{mA}) = \mathbf{320\ mW}$

3. Fixed R_L, Variable V_i

For fixed values of R_L, the voltage V_i must be sufficiently large to turn the Zener diode on. The minimum turn-on voltage $Vi = Vi_{min}$ is determined by

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

and

$$\boxed{V_{i_{min}} = \frac{(R_L + R)V_Z}{R_L}}$$

The maximum value of Vi is limited by the maximum Zener current I_{ZM}. Since $I_{ZM} = I_R - I_L$,

$$\boxed{I_{R_{max}} = I_{ZM} + I_L}$$

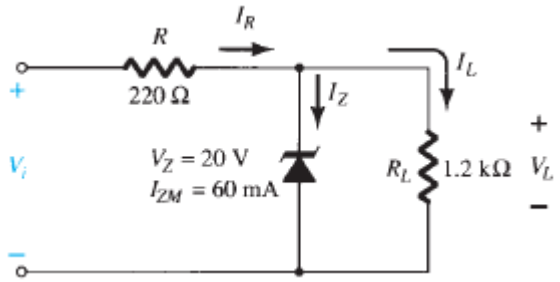
Since I_L is fixed at V_Z / R_L and $I\,ZM$ is the maximum value of I_Z, the maximum Vi is defined by

$$V_{i_{max}} = V_{R_{max}} + V_Z$$

$$\boxed{V_{i_{max}} = I_{R_{max}}R + V_Z}$$

EXAMPLE 13

Determine the range of values of Vi that will maintain the Zener diode in the "on" state.



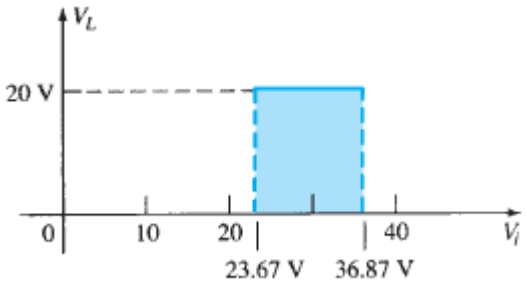
Solution:

$$V_{i_{min}} = \frac{(R_L + R)V_Z}{R_L} = \frac{(1200\ \Omega + 220\ \Omega)(20\ \text{V})}{1200\ \Omega} = \mathbf{23.67\ V}$$

$$I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L} = \frac{20\ \text{V}}{1.2\ \text{k}\Omega} = 16.67\ \text{mA}$$

$$I_{R_{max}} = I_{ZM} + I_L = 60\ \text{mA} + 16.67\ \text{mA}$$
$$= 76.67\ \text{mA}$$

$$V_{i_{max}} = I_{R_{max}}R + V_Z$$
$$= (76.67\ \text{mA})(0.22\ \text{k}\Omega) + 20\ \text{V}$$
$$= 16.87\ \text{V} + 20\ \text{V}$$
$$= \mathbf{36.87\ V}$$



Bipolar Junction Transistors (BJTs)

Basic Construction:

The transistor is a three-layer semiconductor device consisting of either two *n*- and one *p*-type layers of material or two *p*- and one *n*-type layers of material. The former is called an ***npn transistor***, while the latter is called a ***pnp transistor***. Both (with symbols) are shown in Fig. 8-1. The middle region of each transistor type is called the ***base*** (***B***) of the transistor. Of the remaining two regions, one is called ***emitter*** (***E***) and the other is called the ***collector*** (***C***) of the transistor. For each transistor type, a junction is created at each of the two boundaries where the material changes from one type to the other. Therefore, there are two junctions: ***emitter-base (E-B) junction*** and ***collector-base (C-B) junction***. The outer layers of the transistor are heavily doped semiconductor materials having widths much greater than those of the sandwiched *p*- or *n*-type material.

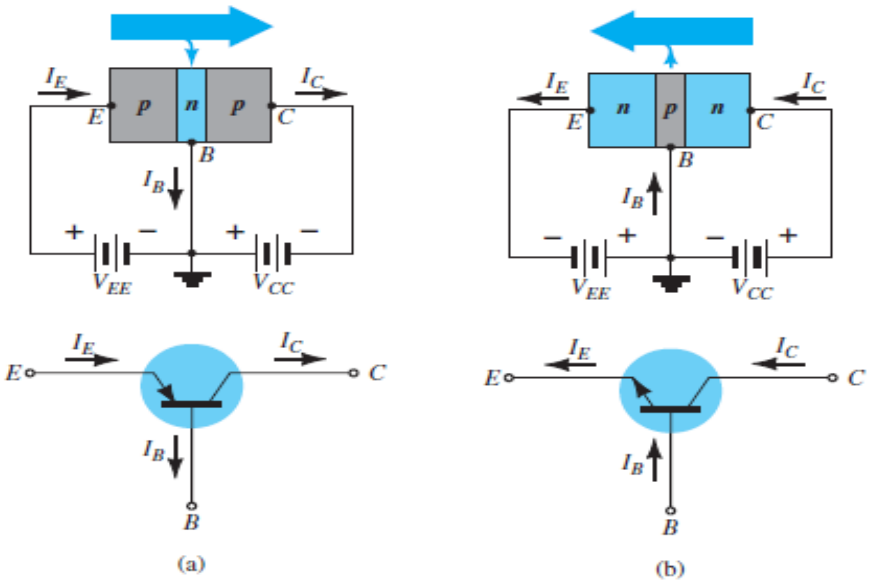


Figure 8-1

The dc biasing is necessary to establish the proper region of operation for ac amplification or switching purposes. Table 8-1 shows the transistor operation regions and the purpose with respect to the biasing of the E-B and C-B junctions.

Table 8-1

Operation region		Purpose	Junctions biasing	
			E-B junction bias	C-B junction bias
1	Active region	Amplification	Forward-biased	Reverse-biased
2	Cutoff region	Switching	Reverse-biased	Reverse-biased
3	Saturation region		Forward-biased	Forward-biased

The abbreviation ***BJT***, from ***bipolar junction transistor***, is often applied to this three-terminal device. The term ***bipolar*** reflects the fact that holes and electrons participate in the injection process into the oppositely polarized material. If only one carrier is employed (electron or hole), it is considered a ***unipolar*** device. Such a device is the ***field-effect transistor*** (***FET***).

Active Region Operation:

The basic operation of the transistor will now be described using the pnp transistor of Fig. 8-2. The operation of the npn transistor is exactly the same if the roles played by the electron and hole are interchanged. When the E-B junction is forward-biased, a large number of majority carriers will diffuse across the forward-biased p-n junction into the n-type material (base). Since the base is very thin and has a low conductivity (lightly doping), a very small number of these carriers will take this path of high resistance to the base terminal. The larger number of these majority carriers will diffuse across the reverse-biased C-B junction into the p-type material (collector). The reason for the relative ease with which the majority carriers can cross the reverse-biased C-B junction is easily understood if we consider that for the reverse-biased diode the injected majority carriers will appear as minority carriers in the n-type base region material. Combining this with the fact that all the minority carriers in the depletion region will cross the reverse-biased junction of a diode accounts for the flow indicated in Fig. 8-2.

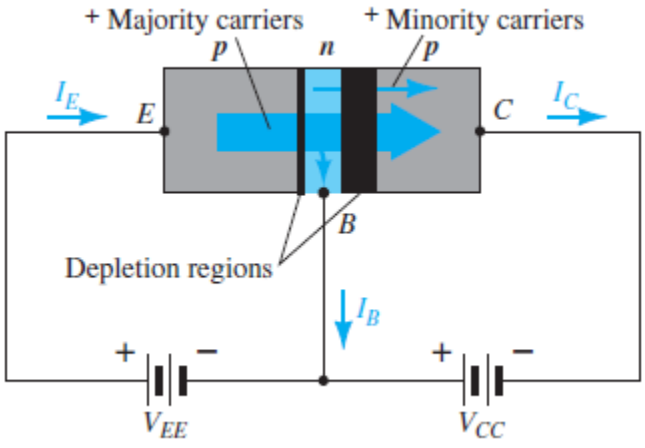


Figure 8-2

Applying Kirchhoff's current law to the transistor of Fig. 8-2, we obtain

$$I_E = I_C + I_B \qquad [8.1]$$

The collector current, however, is comprised of two components: the majority and minority carriers as indicated in Fig. 8-2. The minority-current component is called the ***leakage current*** and is given the symbol I_{CO} (*IC* current with emitter terminal Open). The collector current, therefore, is determined in total by Eq. [8.2].

$$I_C = I_{C\,\text{majority}} + I_{CO\,\text{minority}} \qquad [8.2]$$

Common-Base (CB) Configuration:

The common-base configuration with npn and pnp transistors are indicated in Fig. 8-3. The common-base terminology is derived from the fact that the base is common to both input and output sides of the configuration. In addition, the base is usually terminal closest to, or at, the ground potential.

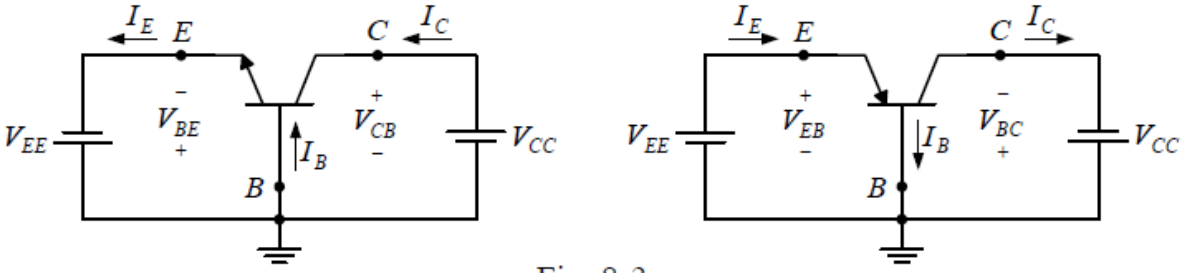


Fig. 8-3

In the dc mode the levels of I_C and I_E due to the majority carriers are related by a quantity called ***alpha*** (α_{dc}) and defined by the following equation:

$$\alpha_{dc} = \frac{I_C}{I_E} \qquad [8.3]$$

Where I_C and I_E are the levels of current at the point of operation and $\alpha_{dc} \approx 1$, or for practical devices: $0.900 \leq \alpha_{dc} \leq 0.998$. Since alpha is defined solely for the majority carriers and from Fig. 8-4, Eq. [8.2] becomes

$$I_C = \alpha I_E + I_{CBO} \qquad [8.4]$$

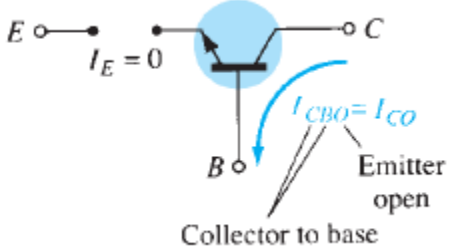


Figure 8-4

The input (emitter) characteristics for a CB configuration are a plot of the emitter (input) current (I_E) versus the base-to-emitter (input) voltage (V_{BE}) for a rage of values of the collector-to-base (output) voltage (V_{CB}) as shown in Fig. 8-5. Since, the exact shape of this I_E-V_{BE} carve will depend on the reverse-biasing output voltage, V_{CB}. The reason for this dependency is that the grater the value of V_{CB}, the more readily minority carriers in the base are swept through the C-B junction. The increase in emitter-to-collector current resulting from an increase in V_{CB} means the emitter current will be greater for a given value of base-to-emitter voltage (V_{BE}).

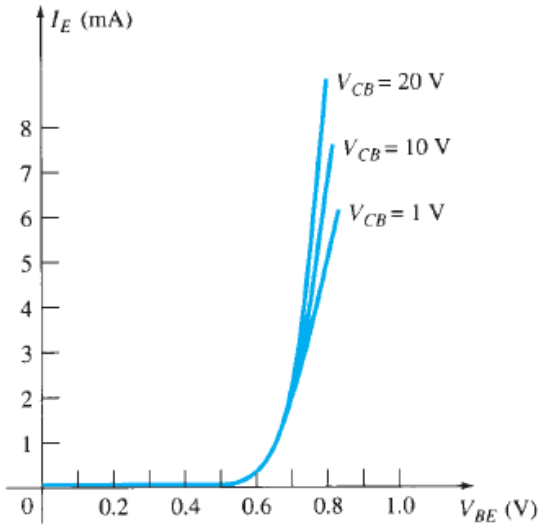


Figure 8-5

The output (collector) characteristics for CB configuration will be a plot of the collector (output) current (I_C) versus collector-to-base (output) voltage (V_{CB}) for a range of values of emitter (input) current (I_E) as shown in Fig. 8-6. The collector characteristics have three basic region of interest, as indicated in Fig. 8-6, the active, cutoff, and saturation regions.

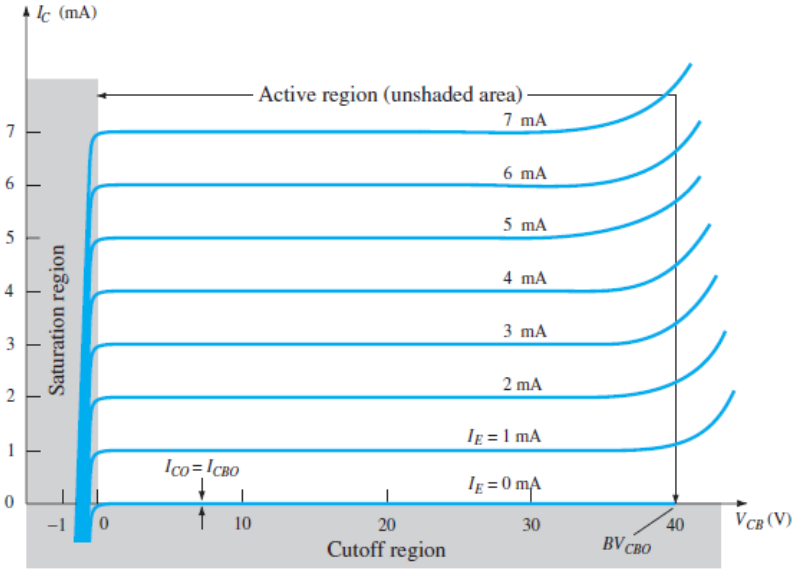


Figure 8-6

- Active region:
  $V_{CB} > 0$ and $I_C = \alpha I_E$.
- Cutoff region:
  $I_E = 0$ and $I_C = I_{CBO}$.
- Saturation region:
  $V_{CB} < 0$ and $I_{C(sat.)} \approx I_{E(sat.)}$.

For ac situations where the point of operation moves on the characteristic carve, an ac alpha (α_{ac}) is defined by

$$\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=const.} \qquad [8.5]$$

The ac alpha is formally called the ***common-base***, ***short-circuit***, ***amplification factor***, and for most situations the magnitudes of α_{ac} and α_{dc} are quite close, permitting the use of the magnitude of one for other.

Fig. 8-7 shows how the common-base output characteristics appear when the effects of breakdown are included. Note the sudden upward swing of each curve at a large value of V_{CB}. The collector-to-base breakdown voltage when $I_E = 0$ (emitter open) is designed BV_{CBO}

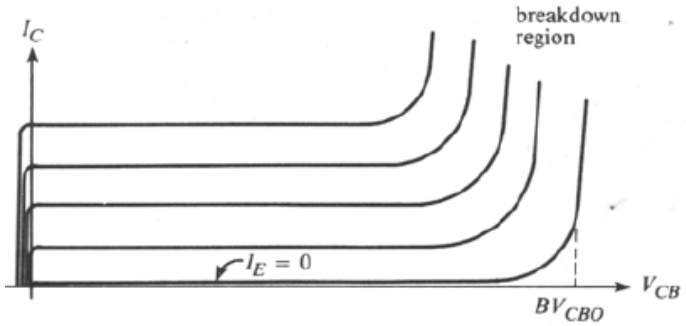


Fig. 8-7

Common-Emitter (CE) Configuration:

The common-emitter configuration with npn and pnp transistors are indicated in Fig. 8-9. The external voltage source V_{BB} is used to forward bias the E-B junction and the external voltage source V_{CC} is used to reverse bias C-B junction. The magnitude of V_{CC} must be greater than V_{BB} to ensure the C-B junction remains reverse biased, since, as can be seen in the Fig.8-9,$V_{CB}=V_{CC}-V_{BB}$.

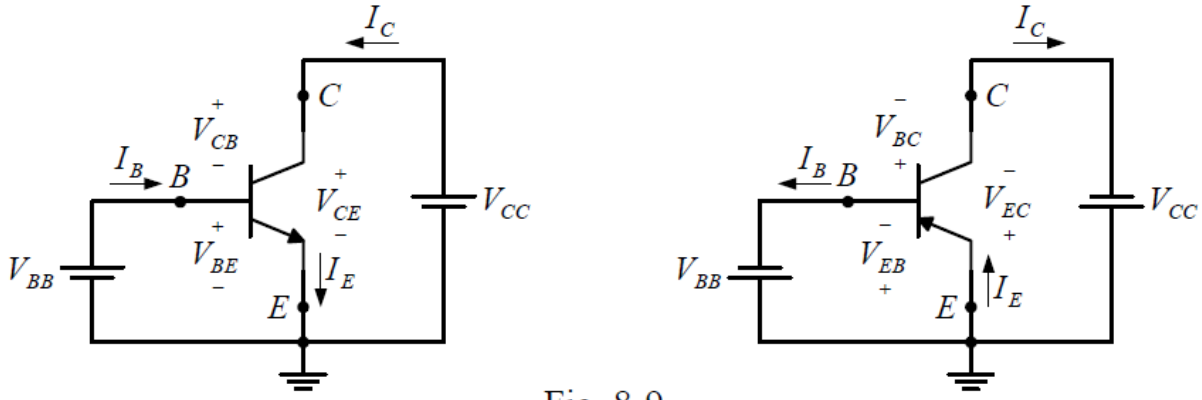


Fig. 8-9

From Eqs. [8.1] and [8.4], we obtain

$$I_C = \alpha(I_C + I_B) + I_{CBO}$$

Rearranging yields

$$I_C = \frac{\alpha I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha} \qquad [8.6]$$

From Fig. 8-10, Eq. [8.6] becomes

$$\boxed{I_{CEO} = \left.\frac{I_{CBO}}{1-\alpha}\right|_{I_B=0}} \qquad [8.7]$$

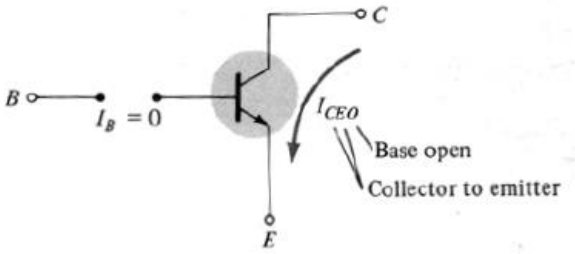


Fig. 8-10

In the dc mode the levels of I_C and I_B are related by a quantity called ***beta*** (β_{dc}) and defined by the following equation:

$$\boxed{\beta_{dc} = \frac{I_C}{I_B}} \qquad [8.8]$$

Where I_C and I_B are the levels of current at the point of operation. For practical devices the levels of β_{dc} typically ranges from about 50 to over 500, with most in the mid-range. On specification sheets β_{dc} is usually included as $\boldsymbol{h_{FE}}$ with *h* derived from an ac ***h***ybrid equivalent circuit.

For ac situation an ac beta (β_{ac}) has been defined as follows:

$$\boxed{\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=const.}} \qquad [8.9]$$

The formal name for β_{ac} is ***common-emitter***, ***forward-current***, ***amplification factor*** and on specification sheets β_{ac} is usually included as $\boldsymbol{h_{fe}}$.

A relationship can be developed between β and α using the basic relationships introduced thus far. Using $\beta = I_C / I_B$ we have $I_B = I_C / \beta$, and from $\alpha = I_C / I_E$ we have $I_E = I_C / \alpha$. Substituting into $I_E = I_C + I_B$ we have $I_C / \alpha = I_C + I_C / \beta$ and dividing both sides of the equation by I_C will result in $1/\alpha = 1 + 1/\beta$ or $\beta = \alpha\beta + \alpha = (\beta + 1)\alpha$ so that

$$\boxed{\alpha = \frac{\beta}{\beta+1} \quad \text{or} \quad \beta = \frac{\alpha}{1-\alpha}} \qquad [8.10]$$

In addition, recall that $I_{CEO} = I_{CBO}/(1-\alpha)$ but using an equivalence of $1/(1-\alpha) = \beta + 1$ derived from the above, we find that $I_{CEO} = (\beta + 1)I_{CBO}$ or

$$\boxed{I_{CEO} \cong \beta I_{CBO}} \qquad [8.11]$$

Beta is particularly important parameter because it provides a direct link between current levels of the input and output circuits for CE configuration. That is,

$$\boxed{I_C = \beta I_B + I_{CEO} \approx \beta I_B} \qquad [8.12]$$

and since $I_E = I_C + I_B = \beta I_B + I_B$ we have

$$\boxed{I_E = (\beta + 1)I_B} \qquad [8.13]$$

The input (base) characteristics for the CE configuration are a plot of the base (input) current (I_B) versus the base-to-emitter (input) voltage (V_{BE}) for a range of values of collector-to-emitter (output) voltage (V_{CE}) as shown in Fig. 8-11. Note that I_B increases as V_{CE} decreases, for a fixed value of V_{BE}. A large value of V_{CE} results in a large reverse bias of the C-B junction, which widens the depletion region and makes the base smaller. When the base is smaller, there are fewer recombination of injected minority carriers and there is a corresponding reduction in base current (I_B).

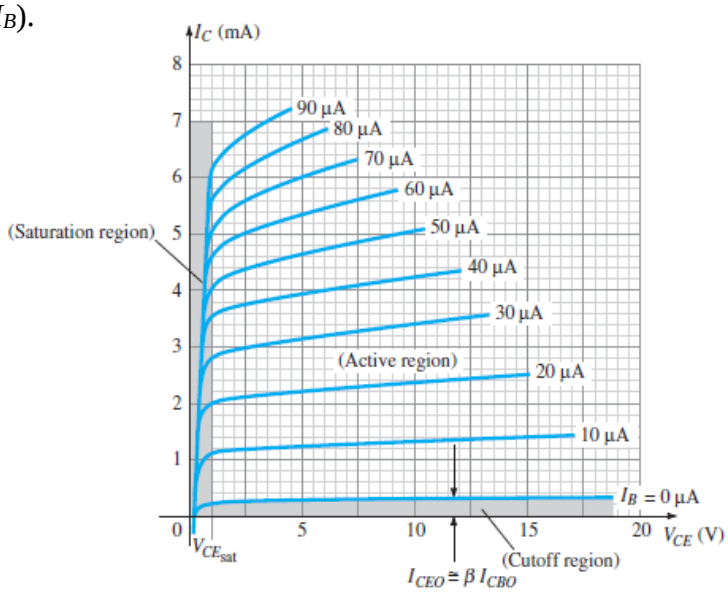


Figure 8-12

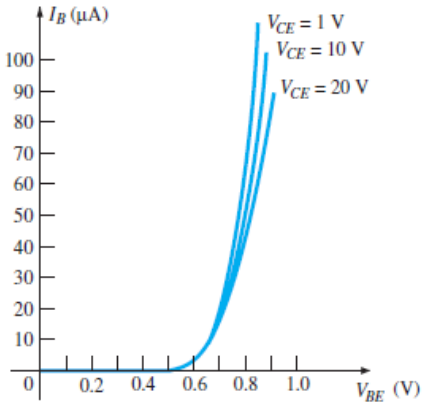


Figure 8-11

The output (collector) characteristics for CE configuration are a plot of the collector (output) current (I_C) versus collector-to-emitter (output) voltage (V_{CE}) for a range of values of base (input) current (I_B) as shown in Fig. 8-12. The collector characteristics have three basic region of interest, as indicated in Fig. 8-12, the active, cutoff, and saturation regions.

- Active region: $I_B > 0$ and $I_C = \beta I_B$.
- Cutoff region: $I_B = 0$ and $I_C = I_{CEO}$.
- Saturation region: $V_{CE} \approx 0$ and $I_{B(sat.)} = I_{C(sat.)} / \beta$.

Common-Collector (CC) Configuration:

The third and final transistor configuration is the common-collector configuration, shown in Fig. 8-13 with npn and pnp transistors. The CC configuration is used primarily for impedance-matching purposes since it has a high input impedance and low output impedance, opposite to that which is true of the common-base and common-emitter configurations.

From a design viewpoint, there is no need for a set of common-collector characteristics to choose the circuit parameters. The circuit can be designed using the common-emitter characteristics. For all practical purposes, the output characteristics of the CC configuration are the same as for the CE configuration. For the CC configuration the output characteristics are a plot of emitter (output) current (I_E) versus collector-to-emitter (output) voltage (V_{CE}), for a range of values of base (input) current (I_B). The output current, therefore, is the same for both the common-emitter and common-collector characteristics. There is an almost unnoticeable change in the vertical scale of I_C of the common-emitter characteristics if I_C is replaced by I_E for the common-collector characteristics (since $\alpha \cong 1$, $I_E \approx I_C$).

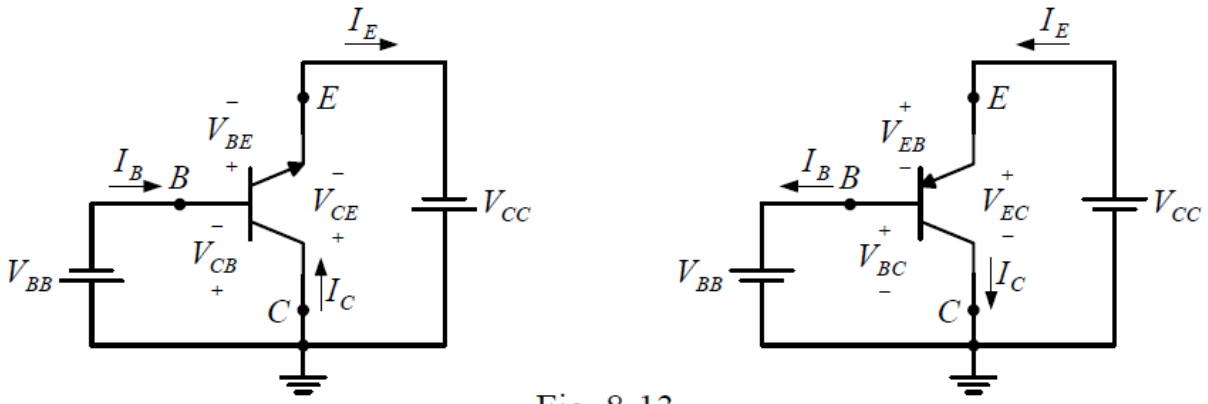


Fig. 8-13

DC Biasing-BJTs

The dc level of operation of a transistor is controlled by a number of factors, including the range of possible operating points on the device characteristics. A network must be constructed that will establish the desired operating point. A number of these networks are analyzed in this chapter. Each design will also determine the stability of the system, that is, how sensitive the system is to temperature variations, another topic to be investigated in a later section of this chapter.

The term *biasing* appearing in the title of this chapter is an all-inclusive term for the application of dc voltages to establish a fixed level of current and voltage. For transistor amplifiers the resulting dc current and voltage establish an *operating point* on the characteristics that define the region that will be employed for amplification of the applied signal. Because the operating point is a fixed point on the characteristics, it is also called the *quiescent point* (abbreviated *Q* -point). By definition, *quiescent* means quiet, still, inactive. Figure 9.1 shows a general output device characteristic with four operating points indicated. The biasing circuit can be designed to set the device operation at any of these points or others within the *active region.* The maximum ratings are indicated on the characteristics of Fig. 9.1 by a horizontal line for the maximum collector current $I_{C\max}$ and a vertical line at the maximum collector-to-emitter voltage $V_{CE\max}$. The maximum power constraint is defined by the curve $P_{C\max}$ in the same figure. At the lower end of the scales are the *cutoff region*, defined by $I_B \leq 0$ mA, and the *saturation region*, defined by $V_{CE} \leq V_{CE\text{sat}}$.

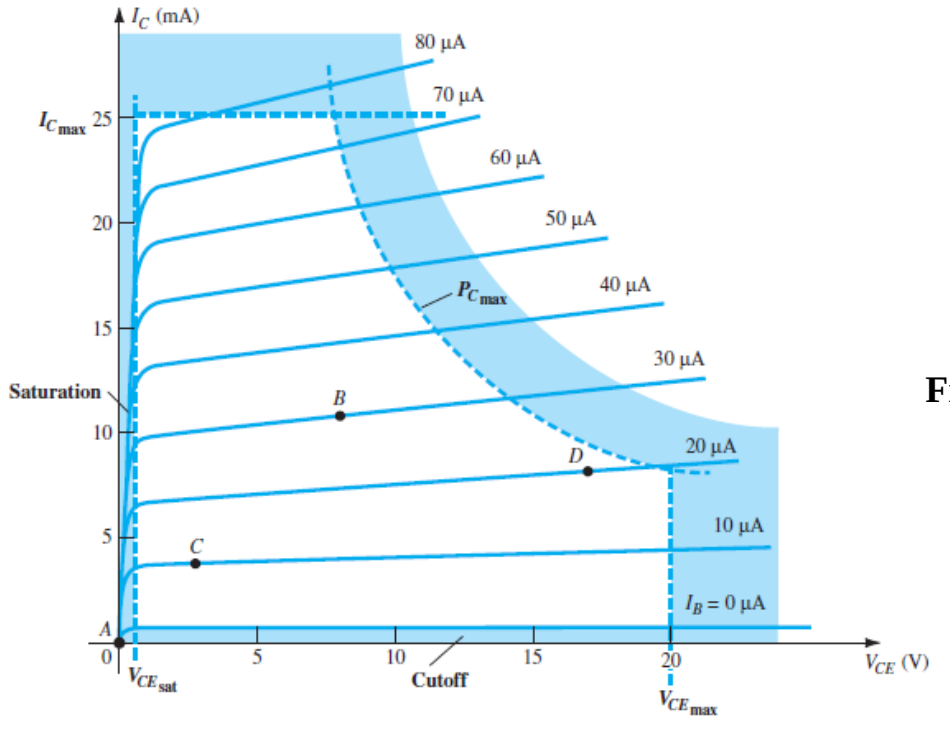


Figure 9-1

Standard Biasing Circuits

1. FIXED-BIAS CONFIGURATION

Fig. 9-2a shows a fixed-bias circuit.

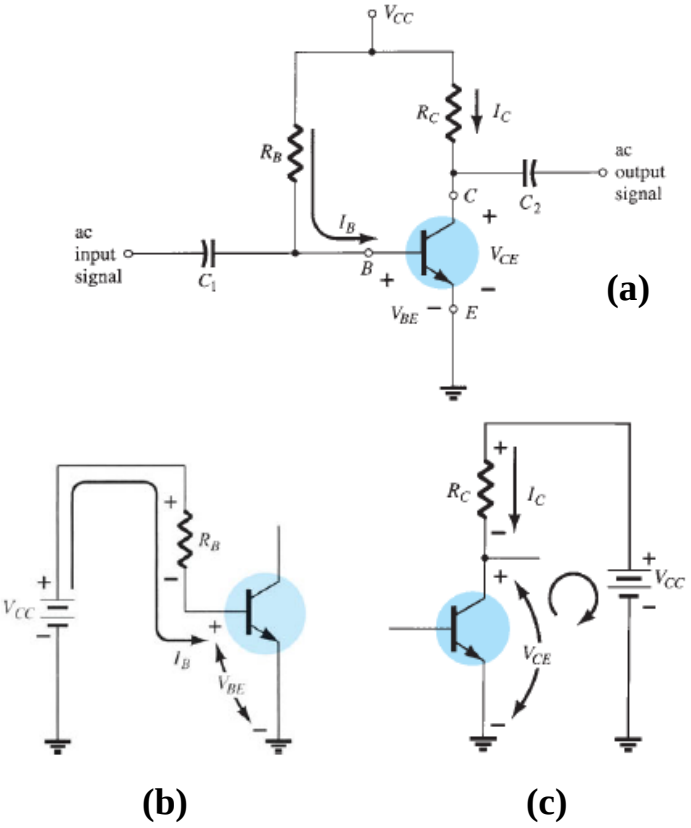


Figure 9-2

Analysis:

- For the input (base-emitter circuit) loop as shown in Fig. 9-2b:

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \qquad [9.1a]$$

- For the output (collector-emitter circuit) loop as shown in Fig. 9-2c:

$$I_C = \beta I_B$$

$$+V_{CE} + I_C R_C - V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C R_C \qquad [9.1b]$$

- For the transistor terminal voltages:

$$V_E = 0V$$
$$V_B = V_{CC} - I_B R_B = V_{BE} \qquad [9.1c]$$
$$V_C = V_{CC} - I_C R_C = V_{CE}$$

Load-Line Analysis:

From Eq. [9.1b] and Fig. 9-3:

- At cutoff region:

$$V_{CE} = V_{CC}\big|_{I_C=0} \qquad [9.2a]$$

- At saturation region:

$$I_C = \frac{V_{CC}}{R_C}\bigg|_{V_{CE}=0} \qquad [9.2b]$$

Design:

For an optimum design:

$$V_{CEQ} = \frac{1}{2}V_{CC}$$
$$I_{CQ} = \frac{1}{2}I_{C(sat)} = \frac{V_{CC}}{2R_C} \qquad [9\text{-}3]$$

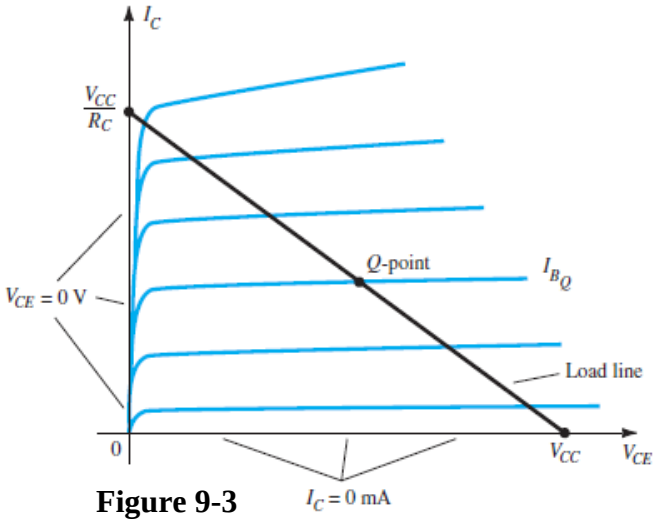


Figure 9-3

2- EMITTER-BIAS CONFIGURATION

Fig. 9-4a shows an emitter-stabilized bias circuit.

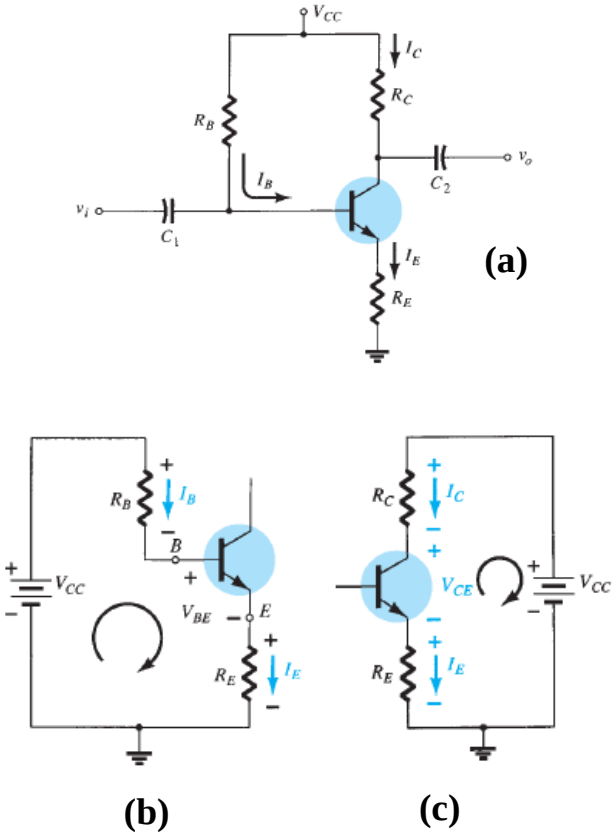


Figure 9-4

Analysis:

- For the input (base-emitter circuit) loop as shown in Fig. 9-4b:

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I_E = (\beta + 1) I_B$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} \qquad [9.4a]$$

- For the output (collector-emitter circuit) loop as shown in Fig. 9-4c:

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

$$I_E \cong I_C$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E) \qquad [9.4b]$$

- For the transistor terminal voltages:

$$V_E = I_E R_E$$

$$V_B = V_{CC} - I_B R_B = V_E + V_{BE} \qquad [9.4c]$$

$$V_C = V_{CC} - I_C R_C = V_E + V_{CE}$$

Load-Line Analysis:

From Eq. [9.4b] and Fig. 9-5:

- At cutoff region:

$$V_{CE} = V_{CC}\big|_{I_C = 0} \qquad [9.5a]$$

- At saturation region:

$$I_C = \frac{V_{CC}}{R_C + R_E}\bigg|_{V_{CE} = 0} \qquad [9.5b]$$

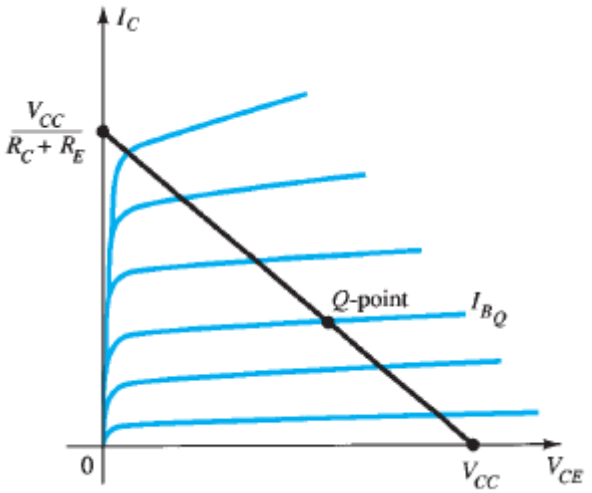


Figure 9-5

Design:

For an optimum design:

$$V_{CEQ} = \frac{1}{2} V_{CC}$$

$$I_{CQ} = \frac{1}{2} I_{C(sat)} = \frac{V_{CC}}{2(R_C + R_E)} \qquad [9\text{-}6]$$

$$V_E = \frac{1}{10} V_{CC}$$

3-VOLTAGE-DIVIDER BIAS CONFIGURATION

Fig. 9-6a shows a voltage-divider bias circuit.

Analyses:

◀ For the input (base-emitter circuit) loop:

Exact Analysis:

From Fig. 9-6b:

$$R_{Th} = R_1 \| R_2 \qquad [9.7a]$$

From Fig. 9-6c:

$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2} \qquad [9.7b]$$

From Fig. 9-6d:

$$+E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$I_E = (\beta + 1) I_B$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E} \qquad [9.7c]$$

$$I_C = \beta I_B$$

Approximate Analysis:

From Fig. 9-6e:

If $R_i >> R_2 \Rightarrow I_2 >> I_B$.

Since $I_B \approx 0 \Rightarrow I_1 \cong I_2$.

Thus R_1 in series with R_2.

That is,

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} \qquad [9.8a]$$

Since $R_i = (\beta + 1) R_E \cong \beta R_E$ the condition that will define whether the approximation approach can be applied will be the following:

$$\beta R_E \geq 10 R_2 \qquad [9.8b]$$

and

$$V_E = V_B - V_{BE}$$

$$I_C \cong I_E = \frac{V_E}{R_E} \qquad [9.8c]$$

◀ For the output (collector-emitter circuit) loop:

$$V_{CE} = V_{CC} - I_C (R_C + R_E) \qquad [9.9]$$

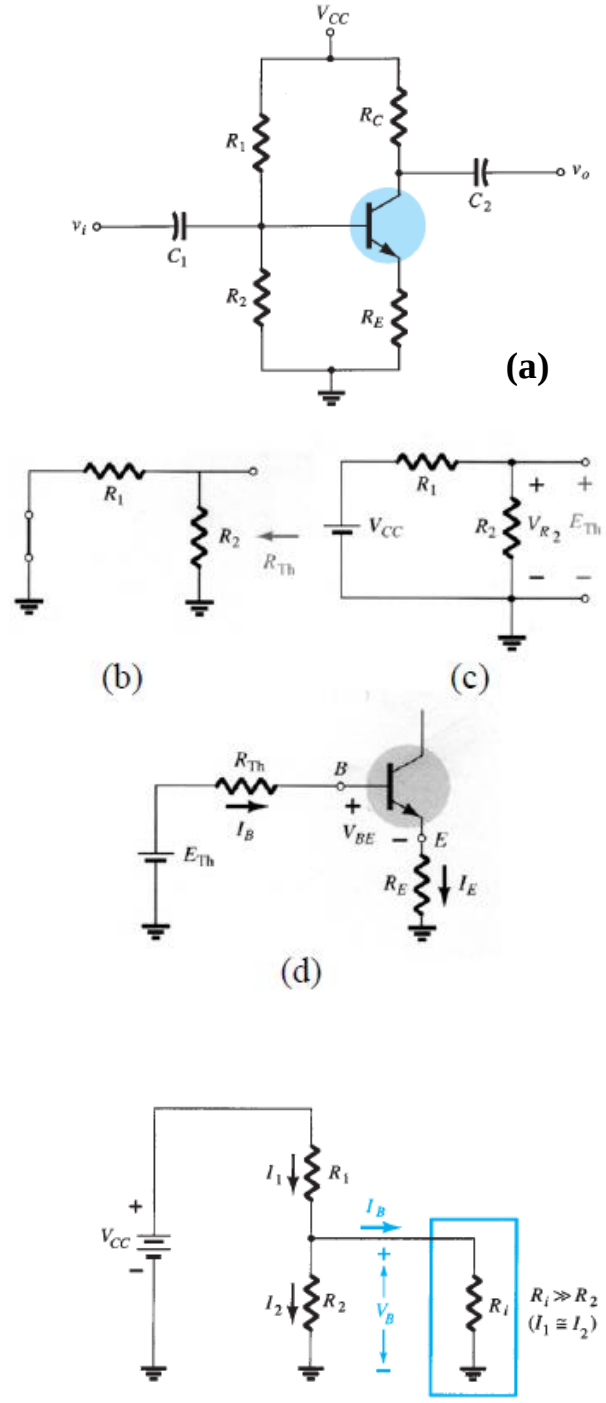


Figure 9-6

Load-Line Analysis:

The similarities with the output circuit of the emitter-biased configuration result in the same intersections for the load line of the voltage-divider configuration. The load line will therefore have the same appearance as that of Fig. 9-5. The level of *IB* is of course determined by a different equation for the voltage-divider bias and the emitter-bias configuration.

Design:

For an optimum design:

$$V_{CEQ} = \frac{1}{2}V_{CC}$$

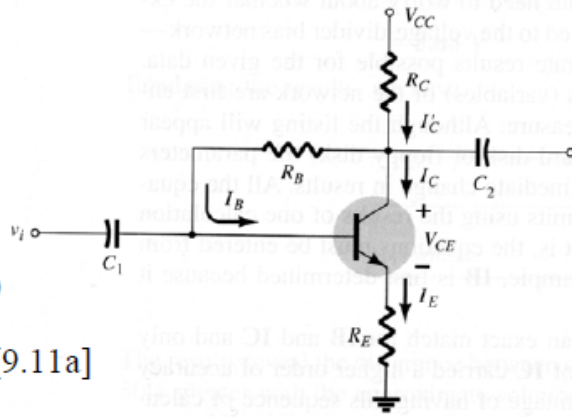
$$I_{CQ} = \frac{1}{2}I_{C(sat)} = \frac{V_{CC}}{2(R_C + R_E)} \qquad [9.10]$$

$$V_E = \frac{1}{10}V_{CC}$$

$$R_2 \leq \frac{1}{10}\beta R_E$$

4-COLLECTOR FEEDBACK CONFIGURATION

Fig. 9-7a shows a voltage-feedback bias circuit.



(a)

Analysis:

◀ For the input (base-emitter circuit) loop as shown in Fig. 9-7b:

$$+V_{CC} - I_C'R_C - I_BR_B - V_{BE} - I_ER_E = 0$$

$$I_C' = I_C + I_B = I_E \cong I_C = \beta I_B$$

$$+V_{CC} - \beta I_BR_C - I_BR_B - V_{BE} - \beta I_BR_E = 0$$

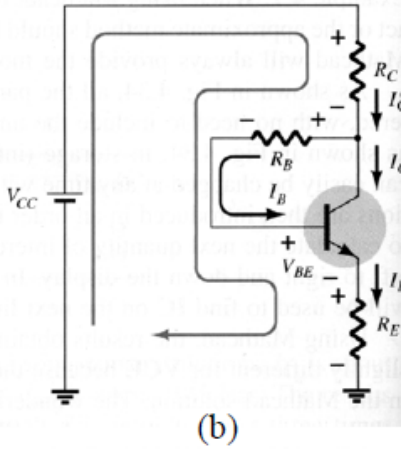
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} \qquad [9.11a]$$

◀ For the output (collector-emitter circuit) loop as shown in Fig. 9-7c:

$$+I_ER_E + V_{CE} + I_C'R_C - V_{CC} = 0$$

$$I_C' = I_E \cong I_C$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \qquad [9.11b]$$



(b)

Load-Line Analysis:

Continuing with the approximation $I_C' = I_C$ will result in the same load line defined for the voltage-divider and emitter-biased configurations. The levels of I_{BQ} will be defined by the chosen base configuration.

Design:

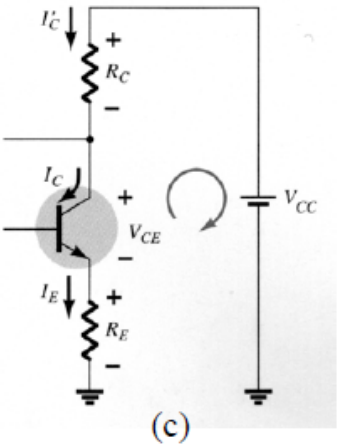
For an optimum design:

$$V_{CEQ} = \frac{1}{2}V_{CC}$$

$$I_{CQ} = \frac{1}{2}I_{C(sat)} = \frac{V_{CC}}{2(R_C + R_E)} \qquad [9\text{-}12]$$

$$V_E = \frac{1}{10}V_{CC}$$

$$R_B \le \beta(R_C + R_E)$$



(c)

Fig. 9-7

BJT AC Analysis

The transistor can be employed as an amplifying device, that mean the output sinusoidal signal is greater than the input sinusoidal signal.

In general, therefore proper amplification design requires that the dc and ac components be sensitive to each other requirements and limitations. In other words, one can make a complete dc analysis of a system before considering the ac response. The key to transistor small-signal analysis is the use of the equivalent circuit (model) to be introduce in this chapter.

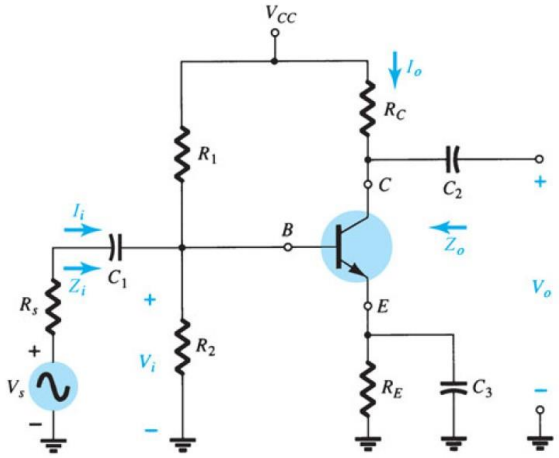
The ac equivalent of a transistor network is obtained by:

1. Setting all dc sources to zero and replacing them by a short-circuit equivalent

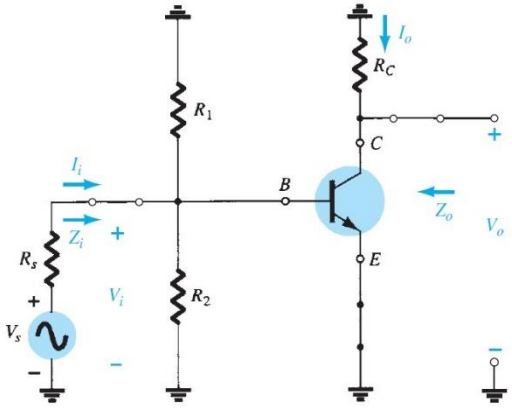
2. Replacing all capacitors by a short-circuit equivalent

3. Removing all elements bypassed by the short-circuit equivalents introduced by steps 1 and 2

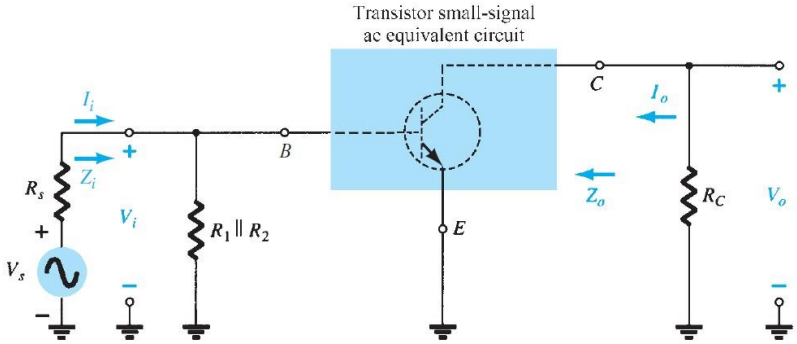
4. Redrawing the network in a more convenient and logical form



-A-



-B-



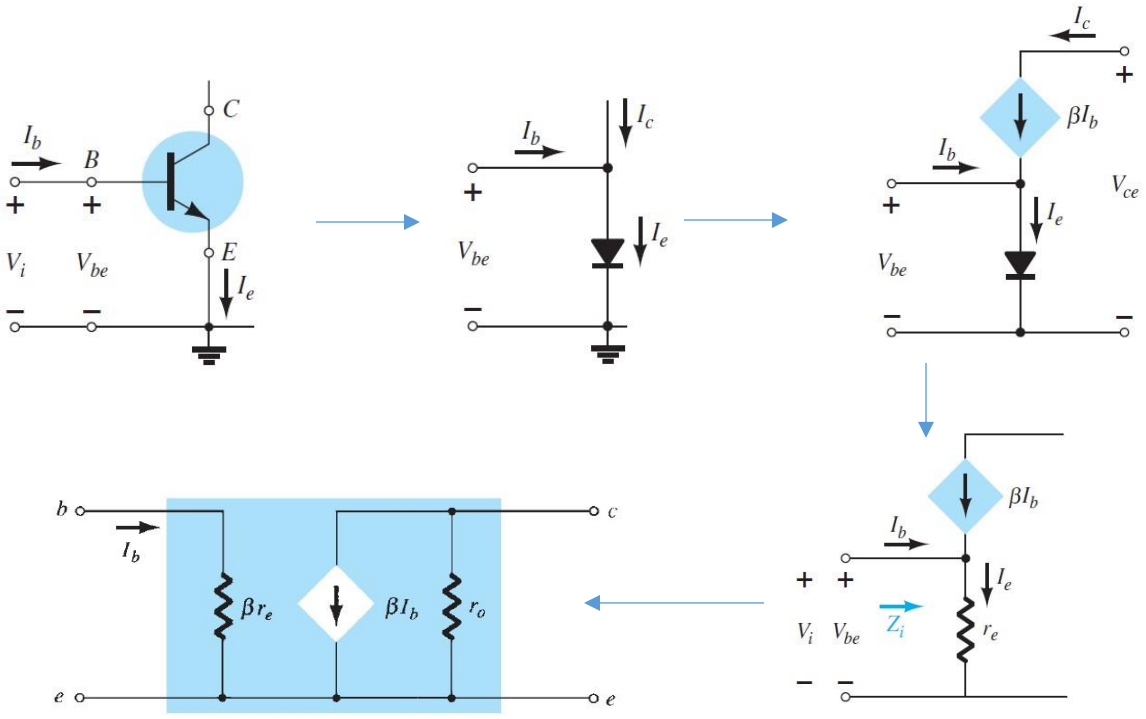
-C-

THE *re* TRANSISTOR MODEL

The *re* model for the CE, CB, and CC BJT transistor configurations will now be introduced with a short description of why each is a good approximation to the actual behavior of a BJT transistor.

A) Common-Emitter Configuration

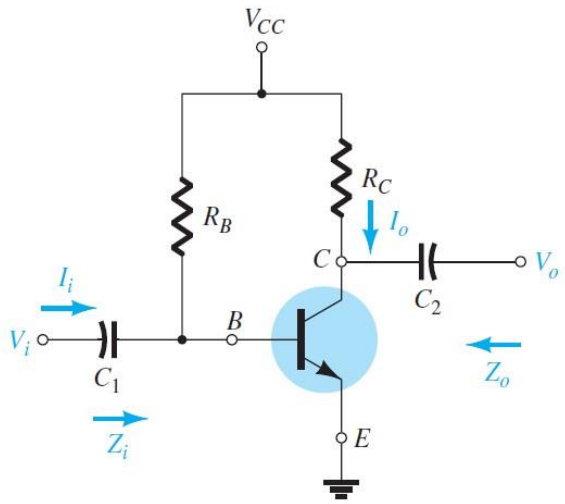
The equivalent circuit for the common-emitter configuration will be constructed using the device characteristics and a number of approximations. Starting with the input side, we find the applied voltage V_i is equal to the voltage *V be* with the input current being the base current I_b as shown:

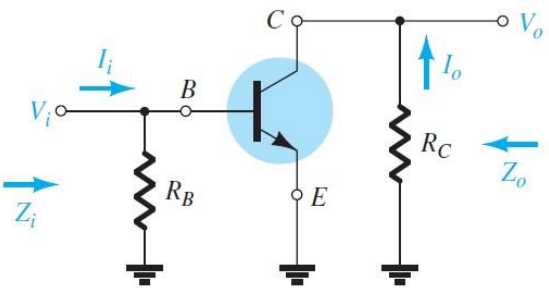


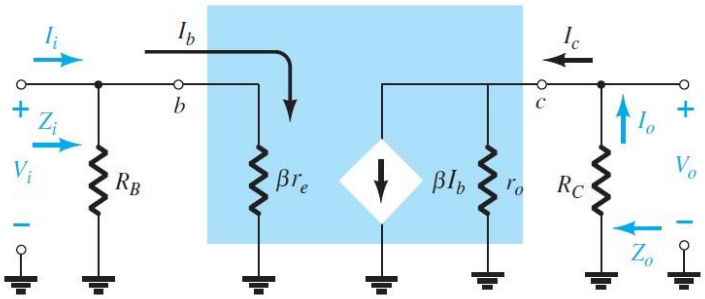
Where:

$$r_e = \frac{26\ mV}{I_E}$$

1- FIXED-BIAS CONFIGURATION







$$Z_i = R_B \| \beta r_e$$

$$Z_i \cong \beta r_e \qquad R_B \geq 10\beta r_e$$

$$Z_o = R_C \| r_o$$

$$Z_o \cong R_C \qquad r_O \geq 10R_C$$

$$V_o = -\beta I_b (R_C \| r_o)$$

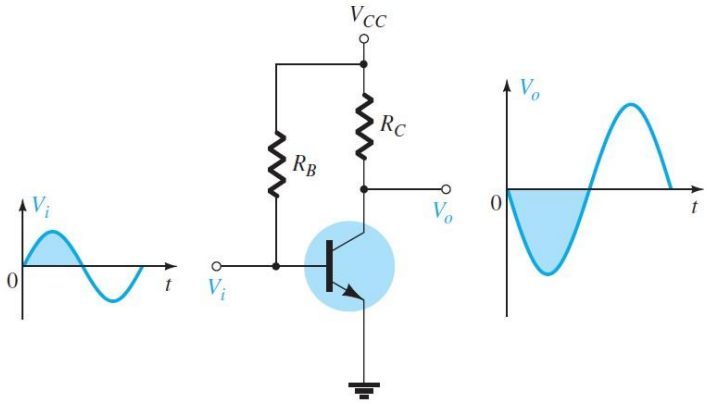
$$I_b = \frac{V_i}{\beta r_e}$$

$$V_o = -\beta \left(\frac{V_i}{\beta r_e} \right) (R_C \| r_o)$$

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{(R_C \| r_o)}{r_e}}$$

$$\boxed{A_v = -\frac{R_C}{r_e}} \qquad r_o \geq 10R_C$$

The negative sign in the resulting equation for A_v reveals that a 180° phase shift occurs between the input and output signals as shown in Fig. below. The is a result of the fact that βI_b establishes a current through R_C that will result in a voltage across R_C, the opposite of that defined by V_o.



Example: for the circuit

a. Determine r_e.
b. Find Z_i (with $r_o = \infty\,\Omega$).
c. Calculate Z_o (with $r_o = \infty\,\Omega$).
d. Determine A_v (with $r_o = \infty\,\Omega$).
e. Repeat parts (c) and (d) including $r_o = 50\,\text{k}\Omega$ in all calculations and compare results.

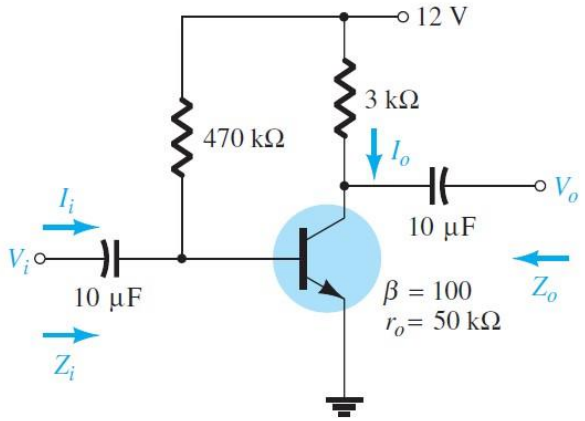


FIG. 5.25
Example 5.1.

Solution:

a. DC analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{470\,\text{k}\Omega} = 24.04\,\mu\text{A}$$

$$I_E = (\beta + 1)I_B = (101)(24.04\,\mu\text{A}) = 2.428\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.428\text{ mA}} = \mathbf{10.71\ \Omega}$$

b. $\beta r_e = (100)(10.71\ \Omega) = 1.071\,\text{k}\Omega$

$$Z_i = R_B \| \beta r_e = 470\,\text{k}\Omega \| 1.071\,\text{k}\Omega = \mathbf{1.07\,k\Omega}$$

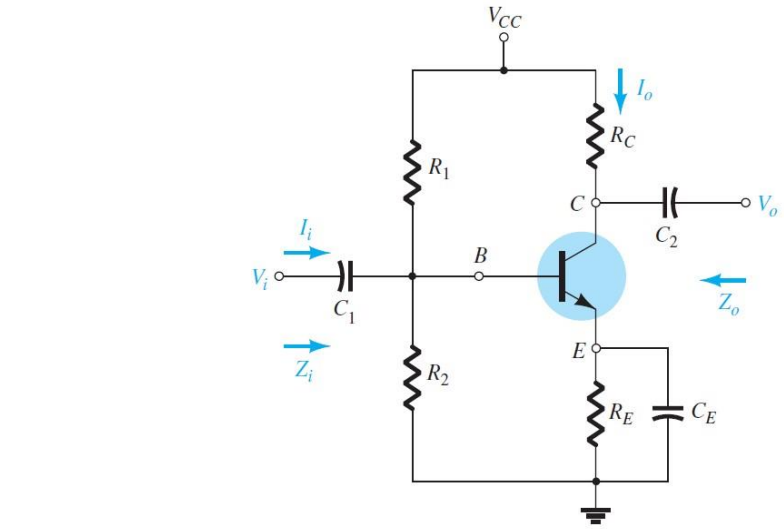
c. $Z_o = R_C = \mathbf{3\,k\Omega}$

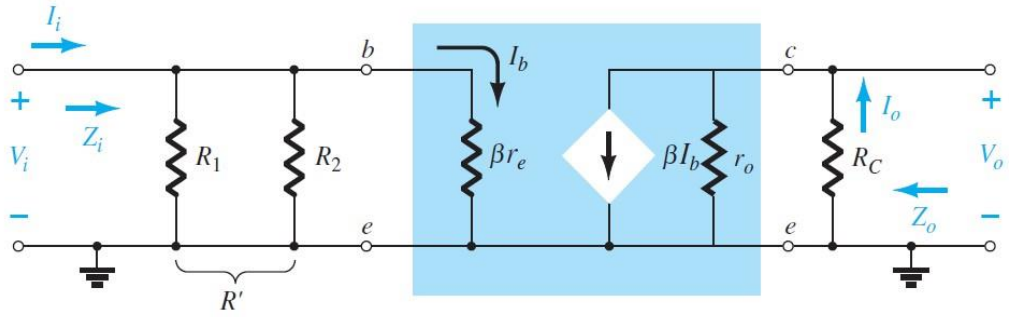
d. $$A_v = -\frac{R_C}{r_e} = -\frac{3\,\text{k}\Omega}{10.71\ \Omega} = \mathbf{-280.11}$$

e. $Z_o = r_o \| R_C = 50\,\text{k}\Omega \| 3\,\text{k}\Omega = \mathbf{2.83\,k\Omega}$ vs. $3\,\text{k}\Omega$

$$A_v = -\frac{r_o \| R_C}{r_e} = \frac{2.83\,\text{k}\Omega}{10.71\ \Omega} = \mathbf{-264.24}\text{ vs. } -280.11$$

2- VOLTAGE-DIVIDER BIAS





$$R' = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$Z_i = R' \| \beta r_e$$

$$Z_o = R_C \| r_o$$

$$Z_o \cong R_C \qquad r_o \geq 10R_C$$

$$V_o = -(\beta I_b)(R_C \| r_o)$$

$$I_b = \frac{V_i}{\beta r_e}$$

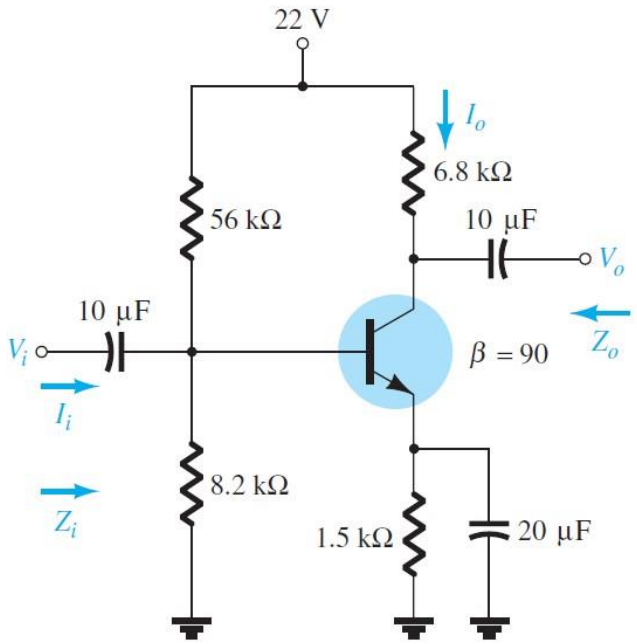
$$V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)(R_C \| r_o)$$

$$A_v = \frac{V_o}{V_i} = \frac{-R_C \| r_o}{r_e}$$

$$A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e} \qquad r_o \geq 10R_C$$

Example: for the circuit

a. r_e.
b. Z_i.
c. Z_o ($r_o = \infty\,\Omega$).
d. A_v ($r_o = \infty\,\Omega$).
e. The parameters of parts (b) through (d) if $r_o = 50\,\text{k}\Omega$ and compare results.



Solution:

a. DC: Testing $\beta R_E > 10R_2$,

$$(90)(1.5\ \text{k}\Omega) > 10(8.2\ \text{k}\Omega)$$

$$135\ \text{k}\Omega > 82\ \text{k}\Omega\ (\textit{satisfied})$$

Using the approximate approach, we obtain

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{(8.2\ \text{k}\Omega)(22\ \text{V})}{56\ \text{k}\Omega + 8.2\ \text{k}\Omega} = 2.81\ \text{V}$$

$$V_E = V_B - V_{BE} = 2.81\ \text{V} - 0.7\ \text{V} = 2.11\ \text{V}$$

$$I_E = \frac{V_E}{R_E} = \frac{2.11\ \text{V}}{1.5\ \text{k}\Omega} = 1.41\ \text{mA}$$

$$r_e = \frac{26\ \text{mV}}{I_E} = \frac{26\ \text{mV}}{1.41\ \text{mA}} = \mathbf{18.44\ \Omega}$$

b. $R' = R_1 \| R_2 = (56\ \text{k}\Omega) \| (8.2\ \text{k}\Omega) = 7.15\ \text{k}\Omega$

$Z_i = R' \| \beta r_e = 7.15\ \text{k}\Omega \| (90)(18.44\ \Omega) = 7.15\ \text{k}\Omega \| 1.66\ \text{k}\Omega$

$= \mathbf{1.35\ k\Omega}$

c. $Z_o = R_C = \mathbf{6.8\ k\Omega}$

d. $A_v = -\frac{R_C}{r_e} = -\frac{6.8\ \text{k}\Omega}{18.44\ \Omega} = \mathbf{-368.76}$

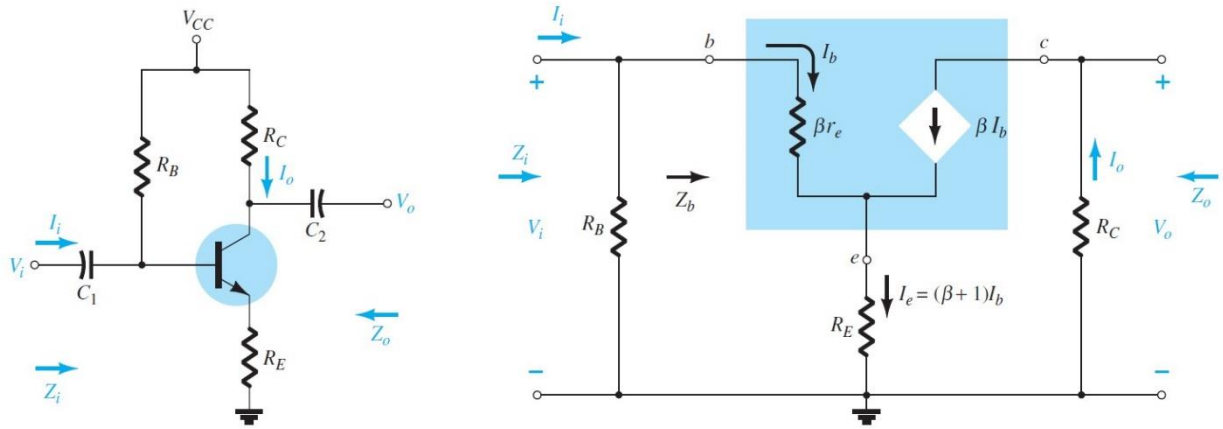
e. $Z_i = \mathbf{1.35\ k\Omega}$

$Z_o = R_C \| r_o = 6.8\ \text{k}\Omega \| 50\ \text{k}\Omega = \mathbf{5.98\ k\Omega}$ vs. $6.8\ \text{k}\Omega$

$A_v = -\frac{R_C \| r_o}{r_e} = -\frac{5.98\ \text{k}\Omega}{18.44\ \Omega} = \mathbf{-324.3}$ vs. -368.76

There was a measurable difference in the results for Z_o and A_v, because the condition $r_o \geq 10R_C$ was *not* satisfied.

3- EMITTER-BIAS CONFIGURATION



Unbypassed (CE وجود عدم **)**

$$V_i = I_b \beta re + I_e R_E$$
$$V_i = I_b \beta re + (\beta+1)\, I_b R_E$$

$$Z_b = \beta r_e + (\beta + 1)R_E$$

Because β is normally much greater than 1, the approximate equation is

$$Z_b \cong \beta(r_e + R_E)$$

Because R_E is usually greater than r_e

$$Z_b \cong \beta R_E$$

$$Z_i = R_B \| Z_b$$

$$Z_o = R_C$$

$$I_b = \frac{V_i}{Z_b}$$

$$V_o = -I_o R_C = -\beta I_b R_C$$

$$= -\beta\left(\frac{V_i}{Z_b}\right)R_C$$

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{\beta R_C}{Z_b}}$$

Substituting $Z_b \approx \beta(re + R_E)$ gives

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e + R_E}}$$

and for the approximation $Z_b \approx \beta R_E$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{R_E}}$$

Effect of r_o

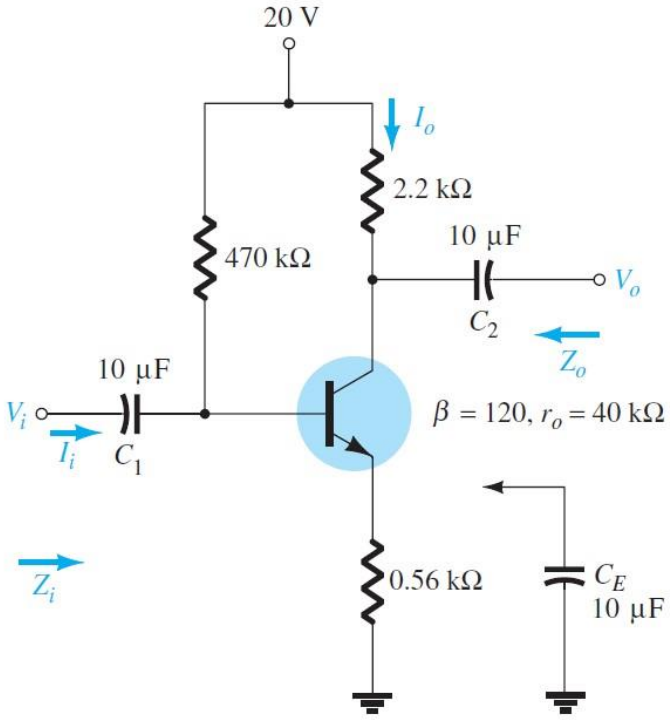
$$\boxed{Z_b \cong \beta(r_e + R_E)} \quad r_o \geq 10(R_C + R_E)$$

$$\boxed{Z_o \cong R_C} \quad \text{Any level of } r_o$$

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{\beta R_C}{Z_b}} \quad r_o \geq 10R_C$$

Examle: For the network

a. r_e.
b. Z_i.
c. Z_o.
d. A_v.



Solution:

a. DC:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{470\text{ k}\Omega + (121)0.56\text{ k}\Omega} = 35.89\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (121)(35.89\ \mu\text{A}) = 4.34\text{ mA}$$

and $$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{4.34\text{ mA}} = \mathbf{5.99\ \Omega}$$

b. Testing the condition $r_o \geq 10(R_C + R_E)$, we obtain

$$40\,\text{k}\Omega \geq 10(2.2\,\text{k}\Omega + 0.56\,\text{k}\Omega)$$
$$40\,\text{k}\Omega \geq 10(2.76\,\text{k}\Omega) = 27.6\,\text{k}\Omega \ (\textit{satisfied})$$

Therefore,

$$Z_b \cong \beta(r_e + R_E) = 120(5.99\,\Omega + 560\,\Omega)$$
$$= 67.92\,\text{k}\Omega$$

and

$$Z_i = R_B \| Z_b = 470\,\text{k}\Omega \| 67.92\,\text{k}\Omega$$
$$= \mathbf{59.34\,k\Omega}$$

c. $Z_o = R_C = \mathbf{2.2\,k\Omega}$

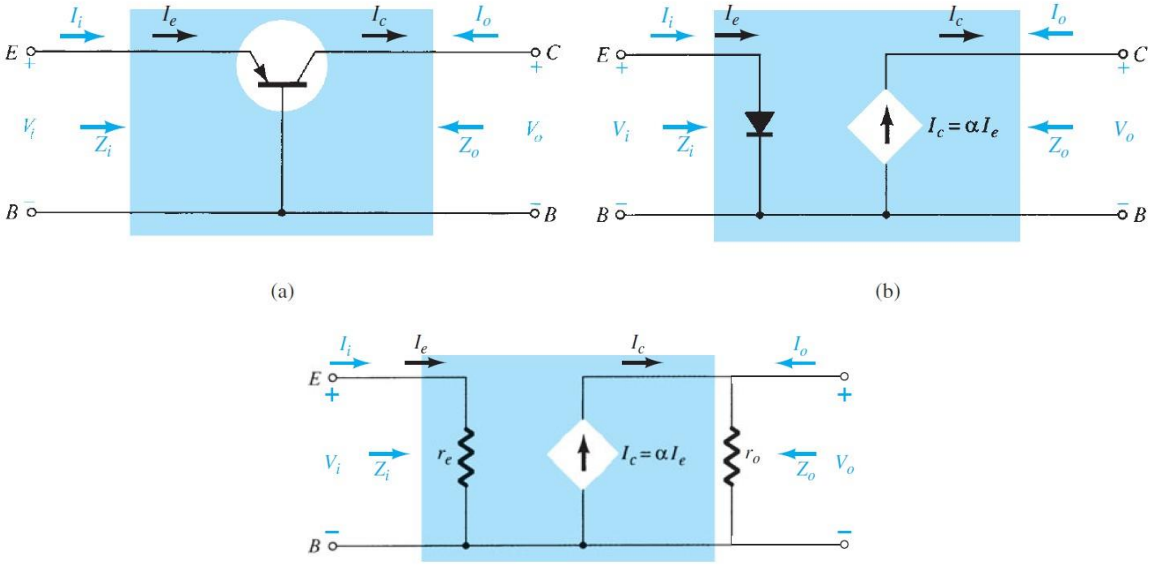
d. $r_o \geq 10R_C$ is satisfied. Therefore,

$$A_v = \frac{V_o}{V_i} \cong -\frac{\beta R_C}{Z_b} = -\frac{(120)(2.2\,\text{k}\Omega)}{67.92\,\text{k}\Omega}$$
$$= \mathbf{-3.89}$$

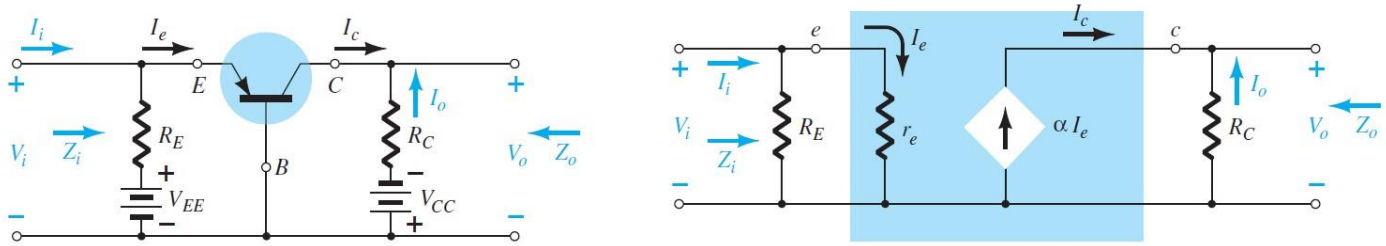
compared to −3.93 using $A_v \cong -R_C/R_E$.

COMMON-BASE CONFIGURATION

The common-base equivalent circuit will be developed in much the same manner as applied to the common-emitter configuration. The general characteristics of the input and output circuit will generate an equivalent circuit that will approximate the actual behavior of the device.



So :



$$Z_i = R_E \| r_e$$

$$Z_o = R_C$$

$$I_e = I_i$$

$$I_o = -\alpha I_e = -\alpha I_i$$

$$V_o = -I_o R_C = -(-I_c)R_C = \alpha I_e R_C$$

$$I_e = \frac{V_i}{r_e}$$

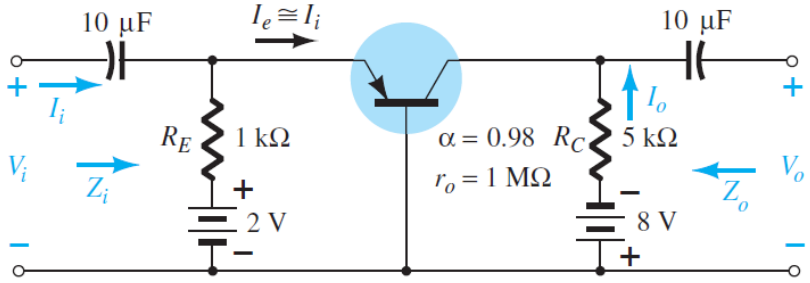
$$V_o = \alpha\left(\frac{V_i}{r_e}\right)R_C$$

$$A_i = \frac{I_o}{I_i} = -\alpha \cong -1$$

$$A_v = \frac{V_o}{V_i} = \frac{\alpha R_C}{r_e} \cong \frac{R_C}{r_e}$$

Example: for the circuit determine

a. r_e.
b. Z_i.
c. Z_o.
d. A_v.
e. A_i.



Solution:

a. $$I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{2\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \frac{1.3\text{ V}}{1\text{ k}\Omega} = 1.3\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{1.3\text{ mA}} = \mathbf{20\ \Omega}$$

b. $$Z_i = R_E \| r_e = 1\text{ k}\Omega \| 20\ \Omega$$

$$= \mathbf{19.61\ \Omega} \cong r_e$$

c. $$Z_o = R_C = \mathbf{5\text{ k}\Omega}$$

d. $$A_v \cong \frac{R_C}{r_e} = \frac{5\text{ k}\Omega}{20\ \Omega} = \mathbf{250}$$

e. $$A_i = \mathbf{-0.98} \cong -1$$

Field-Effect Transistors (FETs)

Basic Definitions:

The FET is a semiconductor device whose operation consists of controlling the flow of current through a semiconductor channel by application of an electric field (voltage).

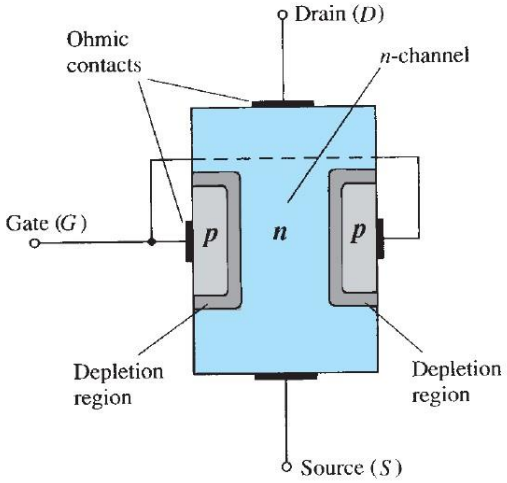
There are two categories of FETs: the ***junction field-effect transistor*** (JFET) and the ***metal-oxide-semiconductor field-effect transistor*** (MOSFET). The MOSFET category is further broken-down into: ***depletion*** and ***enhancement*** types.

A Comparison between FET and BJT:

- FET is a ***unipolar*** device. It operates as a ***voltage-controlled*** device with either electron current in an ***n-channel*** FET or hole current in a ***p-channel*** FET.
- BJT made as ***npn*** or as ***pnp*** is a ***current-controlled*** device in which both electron current and hole current are involved.
- The FET is smaller than a BJT and is thus for more popular in ***integrated circuits*** (ICs).
- FETs exhibit much higher ***input impedance*** than BJTs.
- FETs are more ***temperature stable*** than BJTs.
- BJTs have large ***voltage gain*** than FETs when operated as an amplifier.
- The BJT has a much higher ***sensitivity*** to changes in the applied signal (faster ***response***) than a FET.

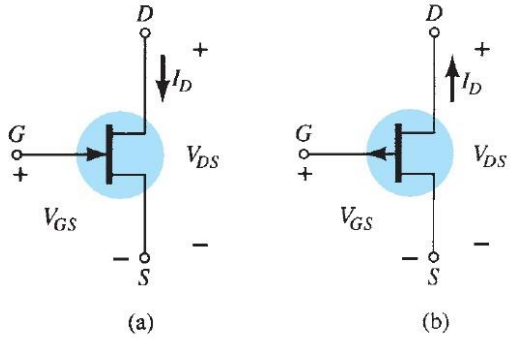
Junction Field-Effect Transistor (JFET):

The basic construction of n-channel JFET is shown in figure below. Note that the major part of the structure is n-type (p-type) material that forms the channel between the embedded layers of p-type (n-type) material. The top of the n-type channel is connected through an ohmic contact to a terminal referred to as the ***drain*** "D", while the lower end of the same material is connected through an ohmic contact to a terminal referred to as the ***source*** "S". The two p-type materials are connected together and to the ***gate*** "G" terminal.



Symbols

The graphic symbols for the *n*-channel and *p*-channel JFETs are provided in figure below. Note that the arrow is pointing in for the *n*-channel device of Fig. a to represent the direction in which I_G would flow if the *p*–*n* junction were forward-biased. For the *p*-channel device Fig. b the only difference in the symbol is the direction of the arrow in the symbol.



Basic Operation of JFET:

1-Bias voltages are shown, in figure below, applied to an n-channel JFET devise.

2-V_{DD} provides a drain-to-source voltage, V_{DS}, (drain is positive relative to source) and supplies current from drain to source, I_D, (electrons move from source to drain).

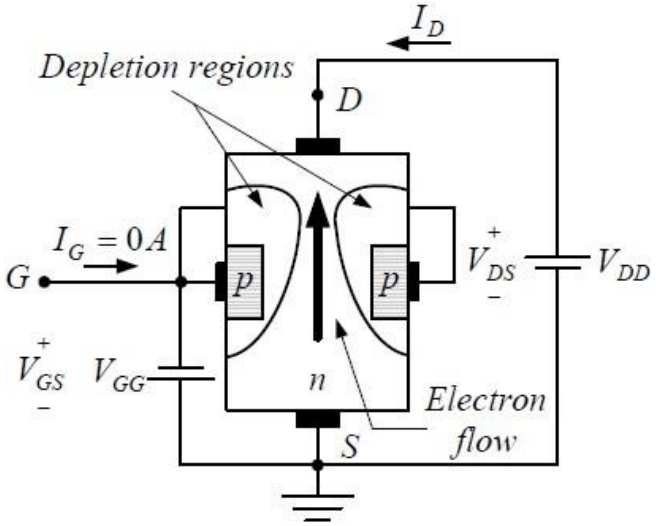
3-V_{GG} sets the reverse-bias voltage between the gate and the source, V_{GS}, (gate is biased negative relative to the source).

4-Input impedance at the gate is very high, thus the gate current I_G = 0 A.

5-Reverse biasing of the gate-source junction produces a depletion region in the n-channel and thus increases its resistance.

6-The channel width can be controlled by varying the gate voltage, and thereby, I_D can also be controlled.

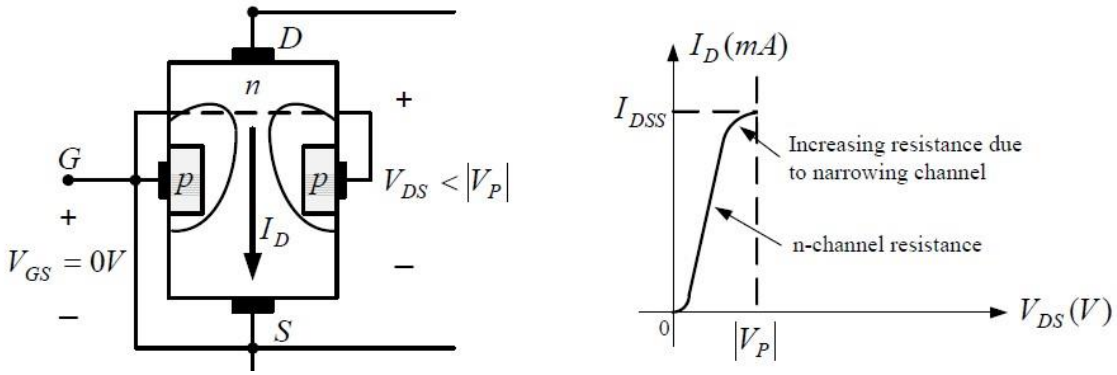
7-The depletion regions are wider toward the drain end of the channel because the reverse-bias voltage between the gate and the drain is grater than that between the gate and the source.



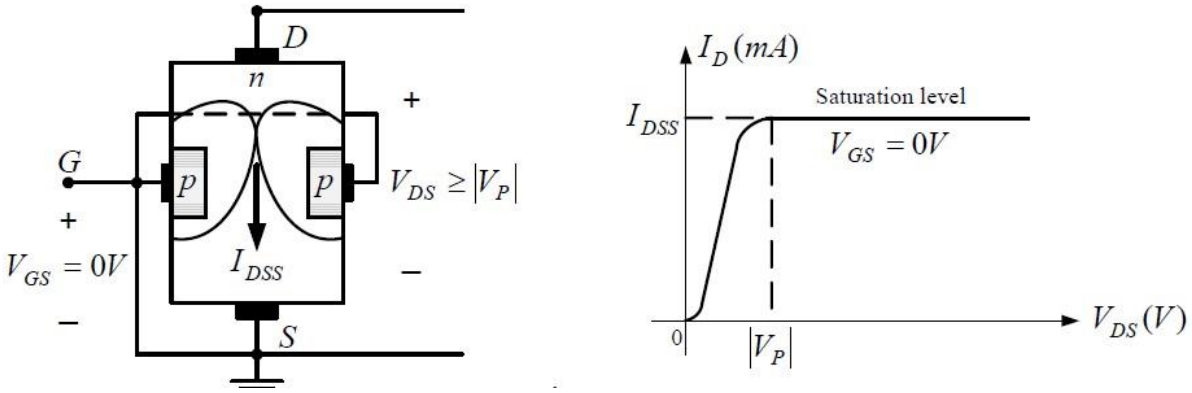
JFET Characteristics

When $V_{GS} = 0$ V and $V_{DS} < V_P$ (***pinch-off voltage***)*: I_D rises linearly with V_{DS} (***ohmic region***, n-channel resistance is constant), as shown in Fig.

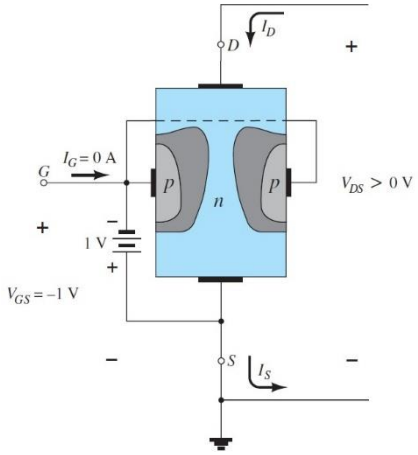
**When V_{DS} is increased to a level where it appears that the two depletion regions would "touch", a condition referred to as pinch-off will result. The level of V_{DS} that establishes this condition is referred to as the pinch-off voltage and is denoted by V_P.*

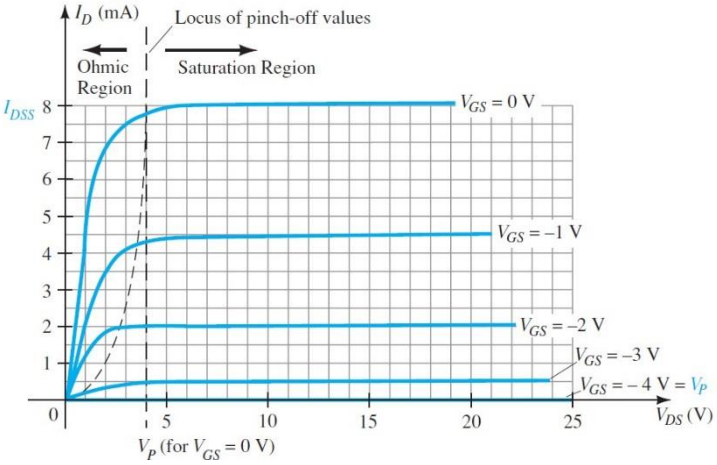


When $V_{GS} = 0$ V and $V_{DS} \geq |V_P|$: I_D remains at its saturation value I_{DSS} beyond V_P, as shown in figure:



When $V_{GS} < 0$ and V_{DS} some positive value: The effect of the applied negative-bias V_{GS} is to establish depletion regions similar to those obtained with $V_{GS} = 0$ V but at lower levels of V_{DS}. Therefore, the result of applying a negative bias to the gate is to reach the saturation level at lower level of V_{DS}, as shown in figure:





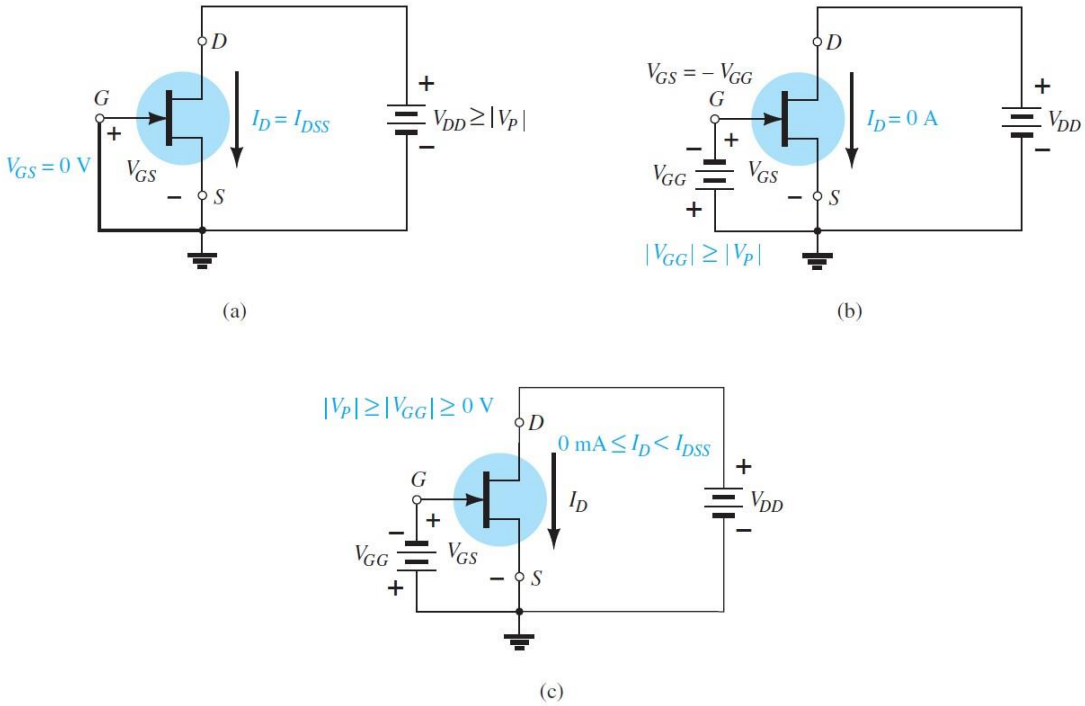
Summary

A number of important parameters and relationships were introduced in this section. A few that will surface frequently in the analysis to follow in this chapter and the next for *n* -channel JFETs include the following:

The maximum current is defined as I_{DSS} and occurs when V_{GS}=0V and $V_{DS} \geq |V_P|$, as shown in Fig. a.

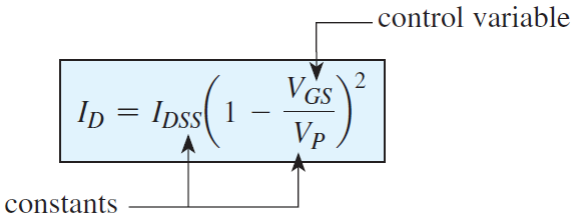
For gate-to-source voltages V_{GS} is less than (more negative than) the pinch-off level, the drain current is 0 A (I_D=0A), as in Fig. b .

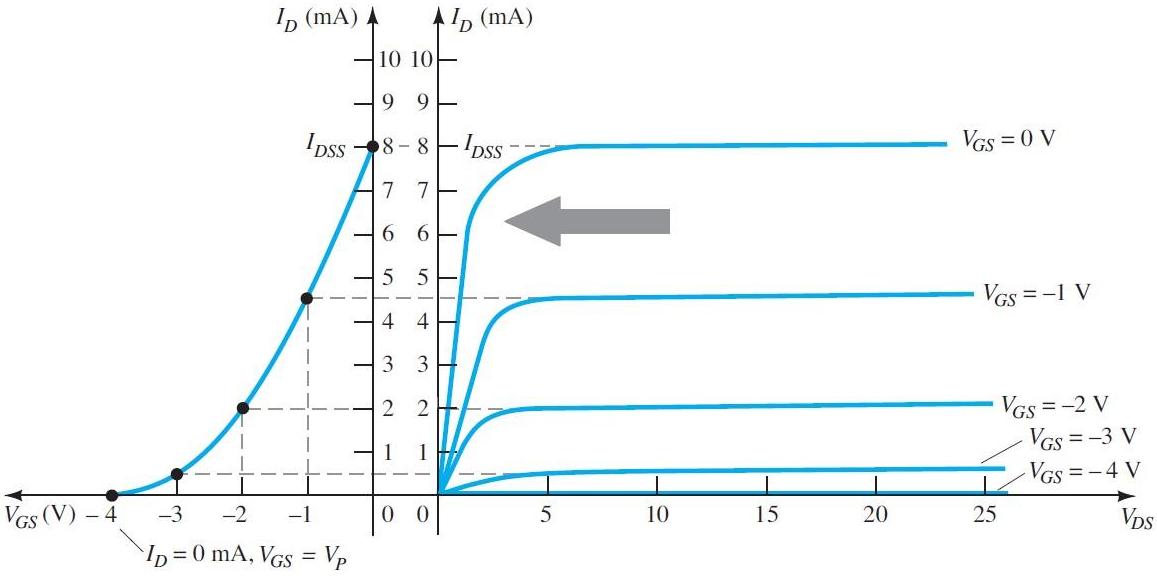
For all levels of V_{GS} between 0 V and the pinch-off level, the current I_D will range between I_{DSS} and 0 A, respectively, as in Fig. c. A similar list can be developed for p-channel JFETs.



(a) $V_{GS} = 0$ V, $I_D = I_{DSS}$; (b) cutoff ($I_D = 0$ A) V_{GS} less than the pinch-off level; (c) I_D is between 0 A and I_{DSS} for $V_{GS} \leq 0$ V and greater than the pinch-off level.

*The transfer characteristics defined by **Shockley's equation** are unaffected by the network in which the device is employed.*





Obtaining the transfer curve from the drain characteristics.

FET DC Biasing

The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$I_G \cong 0\ \text{A}$$

For JFETs

$$I_D = I_S$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

1.FIXED-BIAS CONFIGURATION

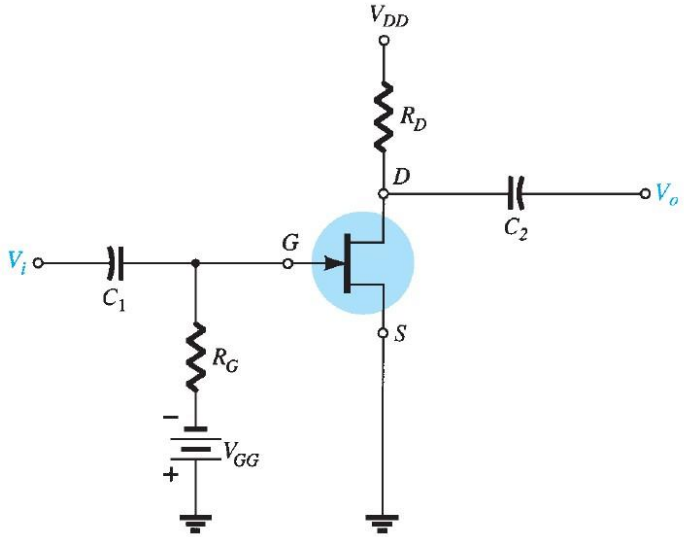
$$V_{GS} = -V_{GG}$$

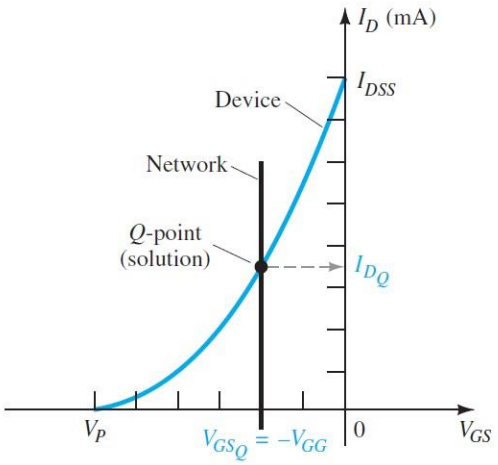
$$V_{DS} = V_{DD} - I_D R_D$$

$$V_S = 0\ \text{V}$$

$$V_D = V_{DS}$$

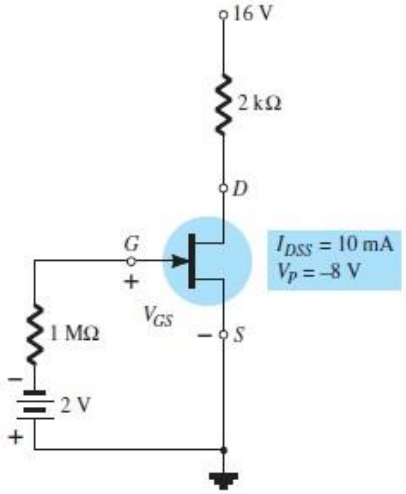
$$V_G = V_{GS}$$





Example: Determine the following for the network:

a. *VGSQ*.
b. *IDQ*.
c. *V DS* .
d. *V D* .
e. *V G* .
f. *V S* .



Solution:

Mathematical Approach

a. $V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$

b. $I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \frac{-2\text{ V}}{-8\text{ V}}\right)^2$
$= 10\text{ mA}(1 - 0.25)^2 = 10\text{ mA}(0.75)^2 = 10\text{ mA}(0.5625)$
$= \mathbf{5.625\ mA}$

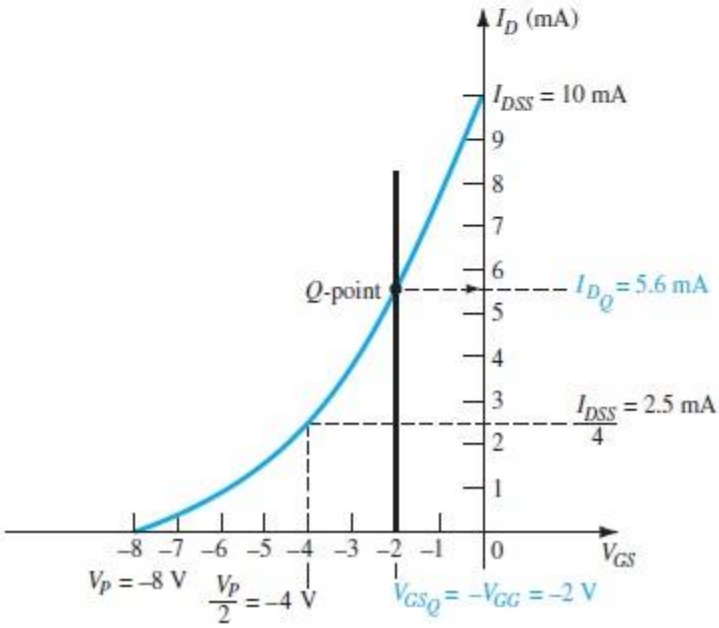
c. $V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.625\text{ mA})(2\text{ k}\Omega)$
$= 16\text{ V} - 11.25\text{ V} = \mathbf{4.75\ V}$

d. $V_D = V_{DS} = \mathbf{4.75\ V}$

e. $V_G = V_{GS} = \mathbf{-2\ V}$

f. $V_S = \mathbf{0\ V}$

Graphical Approach The resulting Shockley curve and the vertical line at $V_{GS} = -2$ V are provided in Fig. 7.7. It is certainly difficult to read beyond the second place without



2-SELF-BIAS CONFIGURATION

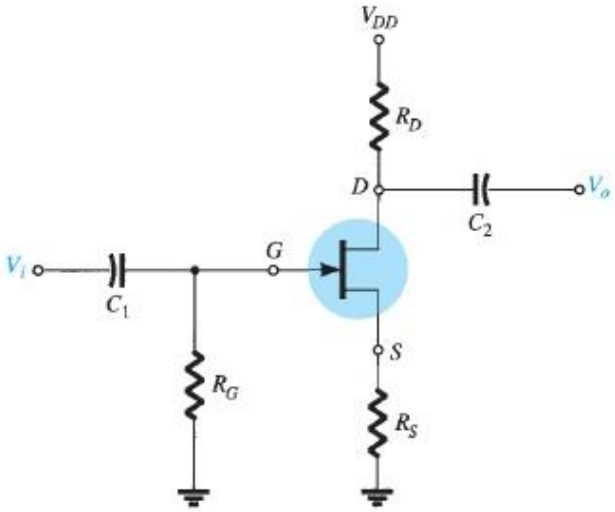
$$V_{GS} = -I_D R_S$$

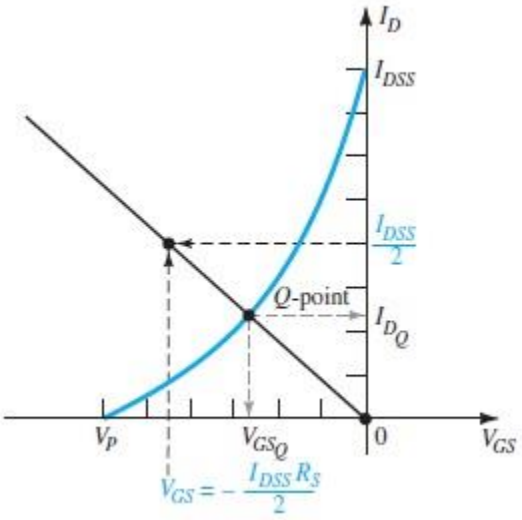
$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$V_S = I_D R_S$$

$$V_G = 0\,\text{V}$$

$$V_D = V_{DS} + V_S = V_{DD} - V_{R_D}$$

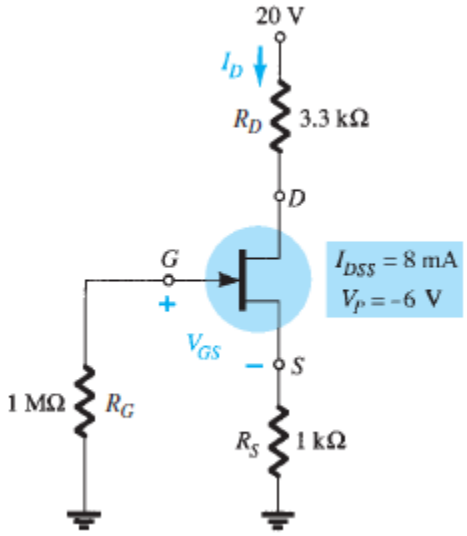




Example:

Determine the following for the network:

a. V_{GSQ}.
b. I_{DQ}.
c. V_{DS}.
d. V_S.
e. V_G.
f. V_D.



Solution:

Choosing $I_D = 4mA$, we obtain

$V_{GS} = -I_D R_S = -(4m)(1k) = -4V$.

At the Q-point

$V_{GSQ} = -2.6V$, and $I_{DQ} = 2.6mA$.

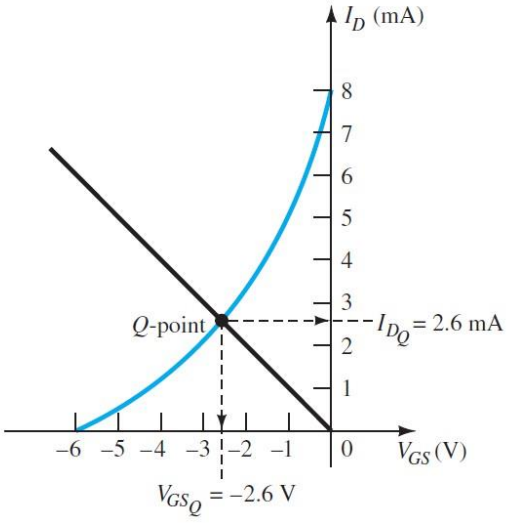
$V_{DS} = V_{DD} - I_D(R_D + R_S)$

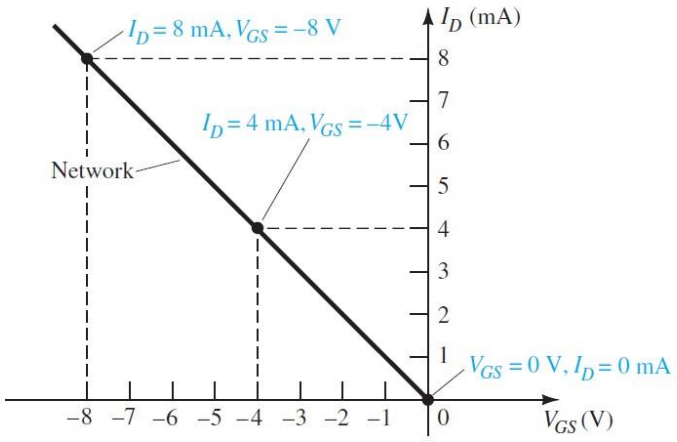
$= 20 - (2.6m)(1k + 3.3k) = 8.82V$.

$V_G = 0V$, and $V_S = I_D R_S = (2.6m)(1k) = 2.6V$.

$V_D = V_{DD} - I_D R_D = 20 - (2.6m)(3.3k) = 11.42V$,

or $V_D = V_{DS} + V_S = 8.82 + 2.6 = 11.42V$.

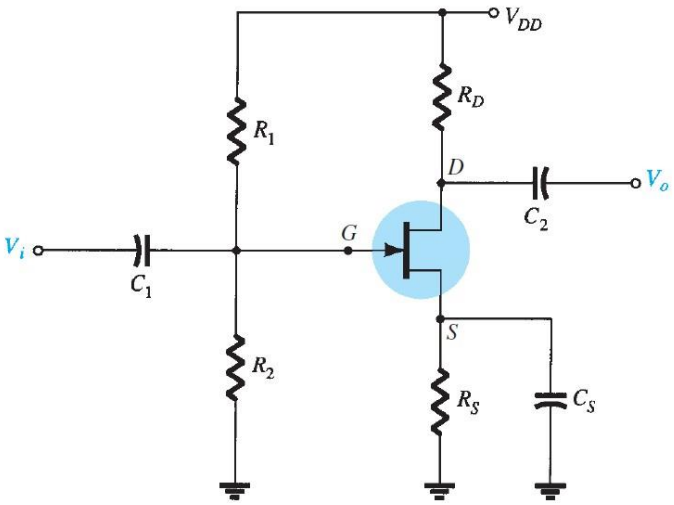




3. VOLTAGE-DIVIDER BIASING

Since $I_G = 0$ *A*

$I_{R1} = I_{R2}$

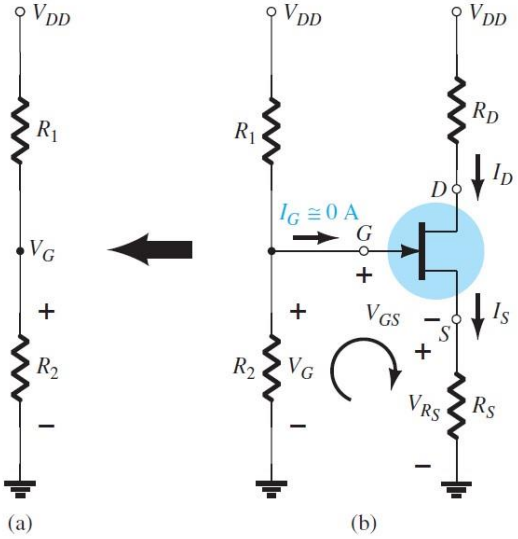


$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$V_G - V_{GS} - V_{RS} = 0$

And $V_{GS} = V_G - V_{RS}$

Substituting $V_{RS} = I_S R_S = I_D R_S$, we have



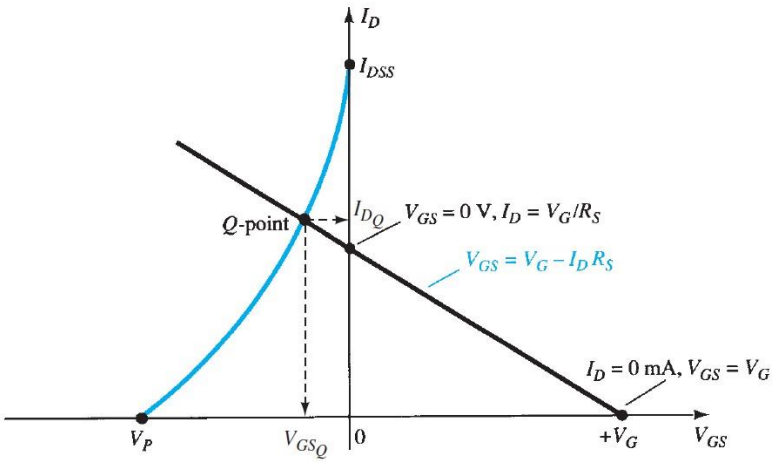
$$V_{GS} = V_G - I_D R_S$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$V_D = V_{DD} - I_D R_D$$

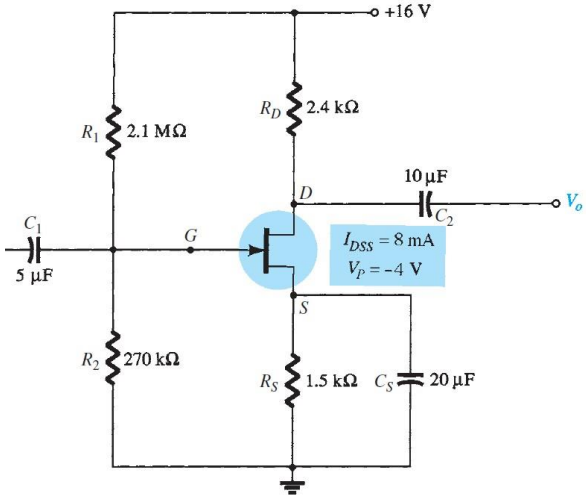
$$V_S = I_D R_S$$

$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}$$



Example: Determine the following for the network

a. I_{DQ} and V_{GSQ}.
b. V_D .
c. V_S .
d. V_{DS} .
e. V_{DG} .



Solution:

a. For the transfer characteristics, if $I_D = I_{DSS}/4 = 8\,\text{mA}/4 = 2\,\text{mA}$, then $V_{GS} = V_P/2 = -4\,\text{V}/2 = -2\,\text{V}$. The resulting curve representing Shockley's equation appears in Fig The network equation is defined by

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

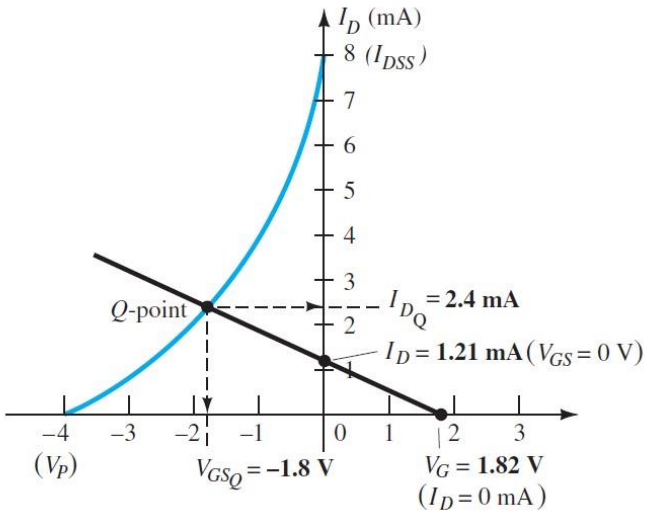
$$= \frac{(270\,\text{k}\Omega)(16\,\text{V})}{2.1\,\text{M}\Omega + 0.27\,\text{M}\Omega}$$

$$= 1.82\,\text{V}$$

and

$$V_{GS} = V_G - I_D R_S$$

$$= 1.82\,\text{V} - I_D(1.5\,\text{k}\Omega)$$



Determining the Q-point for the network

When $I_D = 0$ mA,

$$V_{GS} = +1.82 \text{ V}$$

When $V_{GS} = 0$ V,

$$I_D = \frac{1.82 \text{ V}}{1.5 \text{ k}\Omega} = 1.21 \text{ mA}$$

The resulting bias line appears on Fig. 7.22 with quiescent values of

$$I_{D_Q} = \mathbf{2.4 \text{ mA}}$$

and

$$V_{GS_Q} = \mathbf{-1.8 \text{ V}}$$

b. $V_D = V_{DD} - I_D R_D$

$= 16 \text{ V} - (2.4 \text{ mA})(2.4 \text{ k}\Omega)$

$= \mathbf{10.24 \text{ V}}$

c. $V_S = I_D R_S = (2.4 \text{ mA})(1.5 \text{ k}\Omega)$

$= \mathbf{3.6 \text{ V}}$

d. $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 16 \text{ V} - (2.4 \text{ mA})(2.4 \text{ k}\Omega + 1.5 \text{ k}\Omega)$

$= \mathbf{6.64 \text{ V}}$

or $V_{DS} = V_D - V_S = 10.24 \text{ V} - 3.6 \text{ V}$

$= \mathbf{6.64 \text{ V}}$

e. Although seldom requested, the voltage V_{DG} can easily be determined using

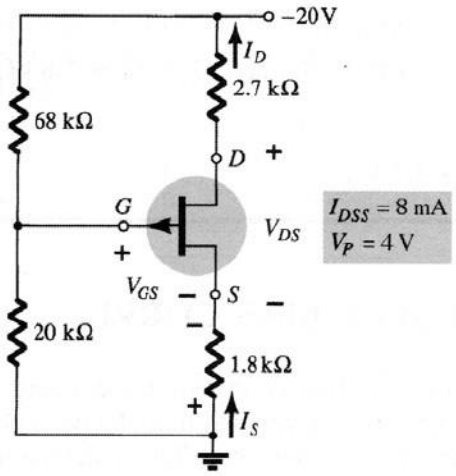
$$V_{DG} = V_D - V_G$$

$$= 10.24 \text{ V} - 1.82 \text{ V}$$

$$= \mathbf{8.42 \text{ V}}$$

Example: (p-channel JFET)

Determine V_{GSQ}, I_{DQ}, and V_{DS} for the p-channel JFET of Fig.



Solution:

$$V_G = \frac{V_{DD} \cdot R_2}{R_1 + R_2} = \frac{(-20)(20k)}{20k + 68k} = -4.55V .$$

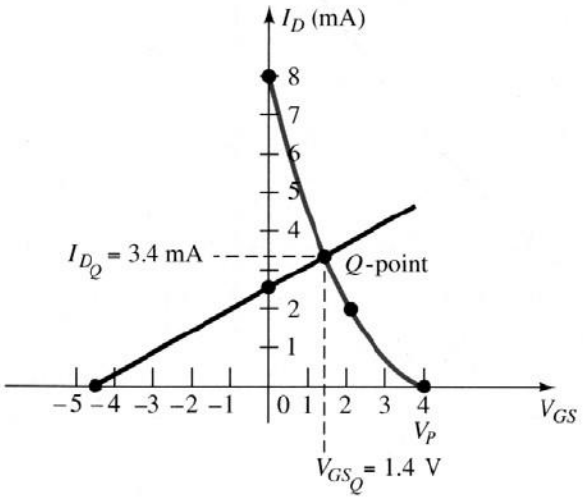
$V_{GS} = V_G + I_D R_S = -4.55 + I_D(1.8k)$,

when $I_D = 0mA$: $V_{GS} = -4.55V$, and

when $V_{GS} = 0V$: $I_D = \frac{-(-4.55)}{1.8k} = 2.53mA$.

At the Q-point (see Fig. 16-17): $V_{GSQ} = 1.4V$, and $I_{DQ} = 3.4mA$.

$V_{DS} = -V_{DD} + I_D(R_D + R_S) = -20 + (3.4m)(2.7k + 1.8) = -4.7V$.

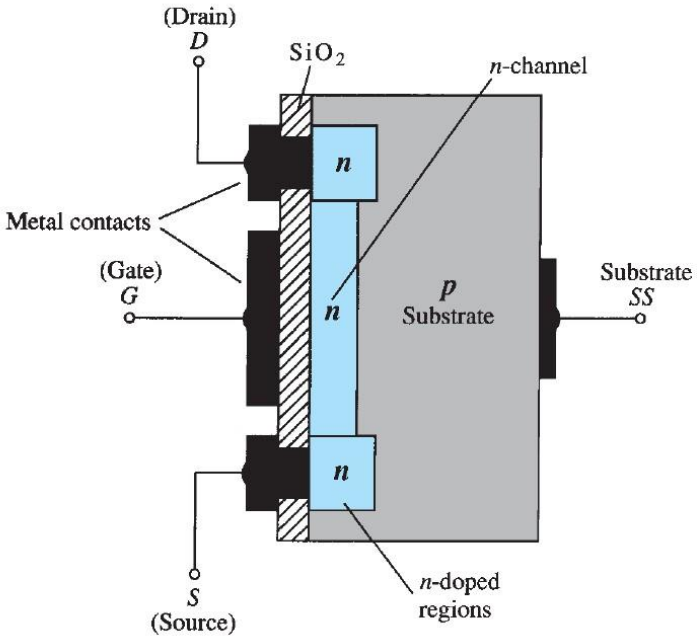


MOSFET

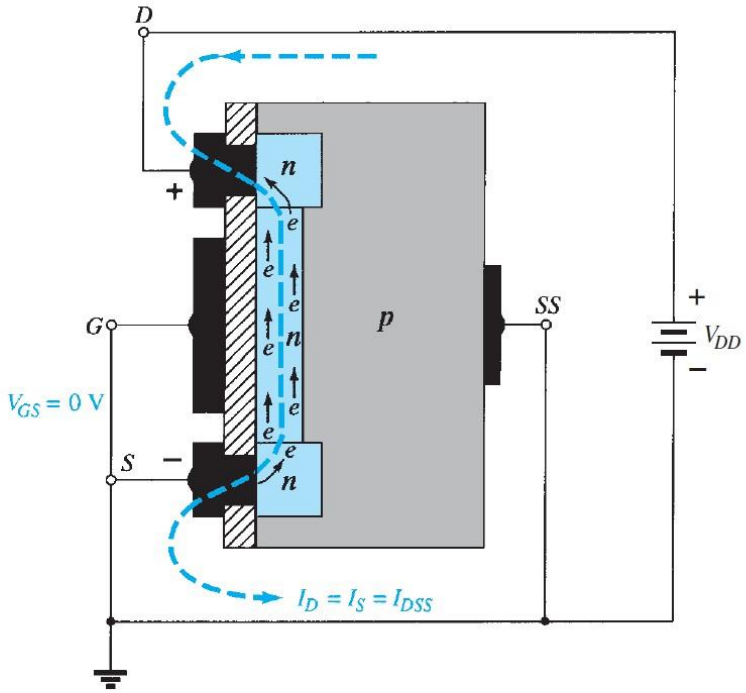
There are three types of FETs: JFETs, MOSFETs, and MESFETs. MOSFETs are further broken down into *depletion type* and *enhancement type.* The terms *depletion* and *enhancement* define their basic mode of operation; the name MOSFET stands for *m*etal –*o*xide– *s*emiconductor *f*ield -*e*ffect *t*ransistor. Since there are differences in the characteristics and operation of different types of MOSFET, they are covered in separate sections. In this section we examine the depletion-type MOSFET, which has characteristics similar to those of a JFET between cutoff and saturation at I_{DSS} , and also has the added feature of characteristics that extend into the region of opposite polarity for V_{GS} .

Basic Construction

There is no direct electrical connection between the gate terminal and the channel of a MOSFET.



Basic Operation and Characteristics



n-Channel depletion-type MOSFET with $V_{GS} = 0$ V and applied voltage V_{DD}.